DESIGN AND ANALYSIS OF 2:1 MULTIPLEXER CIRCUITS FOR HIGH PERFORMANCE

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ABSTRACT

A multiplexer is a unidirectional device and used in any application in which data must be switched from multiple sources to a destination. The low power circuits have become a top priority in modern VLSI design. This paper presents the power consumption comparisons and delay of various designs of 2:1 Multiplexer. The various logic styles such as Differential Cascode Voltage Switch Logic (DCVSL), Modified Differential Cascode voltage switch logic (MDCVSL), CMOS logic and Pseudo NMOS Logic, these designs are analyzed using the Tanner EDA tool. The Pseudo NMOS Logic design demonstrates its superiority against other styles of 2:1 multiplexer design in terms of power consumption.

Keywords: CMOS Logic, DCVSL, MDCVSL, Low power, 2:1 Multiplexer and VLSI.

I INTRODUCTION

In electronics, a multiplexer is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2^n inputs has 'n' select lines, which are used to select which input line to send to the output. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A multiplexer is also called a data selector. An electronic multiplexer makes it possible for several signals to share one device or resource, for example one A/D converter or one communication line, instead of having one device per input signal.

An electronic multiplexer can be considered as a multiple-input, single-output switch, and a demultiplexer as a single-input, multiple-output switch. The schematic symbol for a multiplexer is an isosceles trapezoid with the longer parallel side containing the input pins and the short parallel side containing the output pin. The schematic on the right shows a 2-to-1 multiplexer on the left and an equivalent switch on the right. The wire connects the desired input to the output. The basic function of a multiplexer: combining multiple inputs into a single data stream. Multiplexers can also be used as programmable logic devices. By specifying the logic arrangement in the input signals, a custom logic circuit can be created. The selector inputs then act as the logic inputs.This is especially useful in situations when cost is a factor and for modularity. Therefore study on multiplexer is inevitable [1].

II. LITERATURE REVIEW OF DIFFERENT 2:1MULTIPLEXER CIRCUITS

2.1. DCVSL Multiplexer Circuit

Cascode Voltage Switch Logic (CVSL) refers to a CMOS-type logic family which is designed for certain advantages. This logic family is also known as Differential Cascode Voltage Switch Logic (DCVS or DCVSL).It requires mainly N-channel MOSFET transistors to implement the logic using true and complementary input signals, and also needs two P-channel transistors at the top to pull one of the outputs high.In this paper, we explore the Differential Cascode Voltage-Switch Logic (DCVSL) circuit design methodology. The key benefits of DCVSL are consumes no static power, uses latch to compute output quickly, requires true/complement inputs, produces true/complement outputs [2]-[4]. Allows "Complex" gates, never needs inverters in the logic path and low power consumption. A logic function and its inverse are automatically implemented in this logic style [4], [5].The schematic diagram of DCVSL 2:1 multiplexer is shown in Fig.1. The pull-down network implemented by the NMOS logic tree generates complementary output. This logic family is also known as Differential Cascode Voltage Switch Logic (DCVS or DCVSL).The advantage of DCVSL is in its logic density that is achieved by elimination of large PFETS from each logic function. It can be divided it to two basic parts: a differential latching circuit and a cascoded complementary logic array [6]-[10].

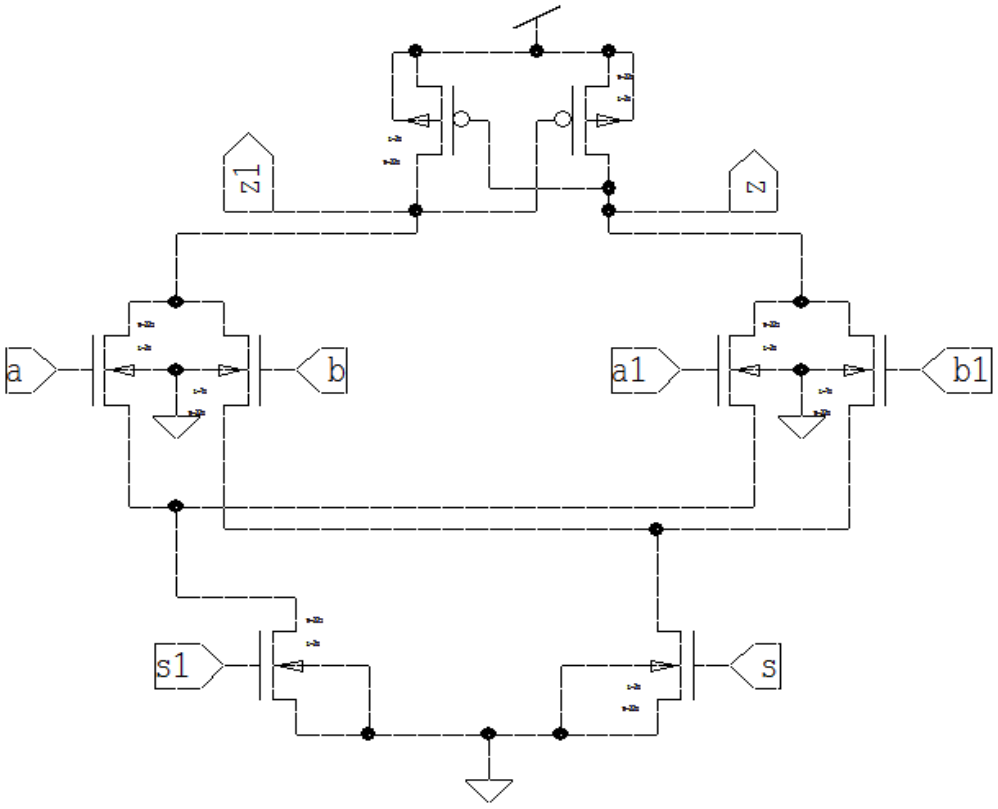

Fig. 1 Schematic of DCVSL Circuit

2.2. MDCVSL Multiplexer Circuit

Adding two NMOS transistors in the pull up part of Differential Cascode Voltage-Switch Logic (DCVSL) 2:1 multiplexer the circuit shows a remarkable improvement over the existing design. In the proposed circuit due to the excess added transistors there is a reduction in threshold loss for the circuit, which further causes the reduction in overall power consumption of the circuit. Due to the transmission gate topology in this design the circuit shows better output waveforms in terms of threshold loss. The two logic trees are capable of processing complex functions within a single circuit delay. The schematic of Modified Differential Cascode Voltage-Switch Logic (MDCVSL) design of 2:1 multiplexer is shown in Fig.2.

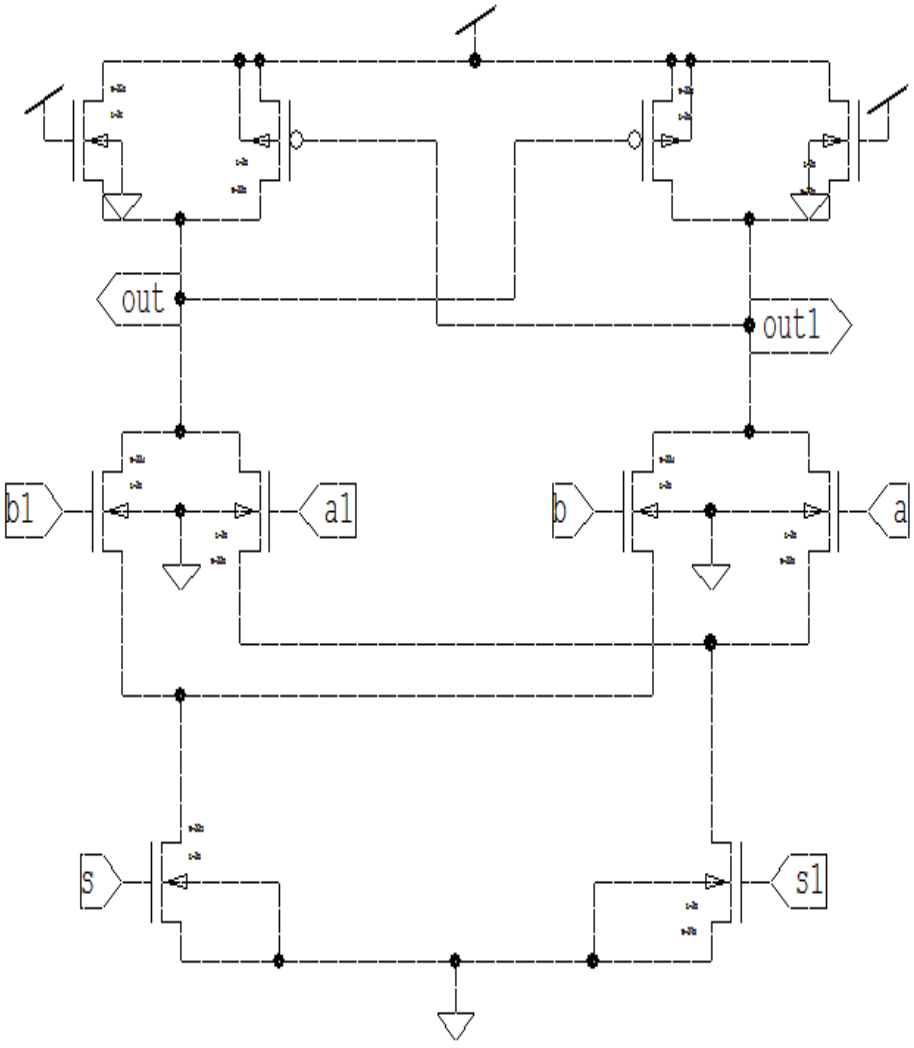

Fig. 2 Schematic of DCVSL circuit

2.3. CMOS Logic Based Multiplexer Circuit

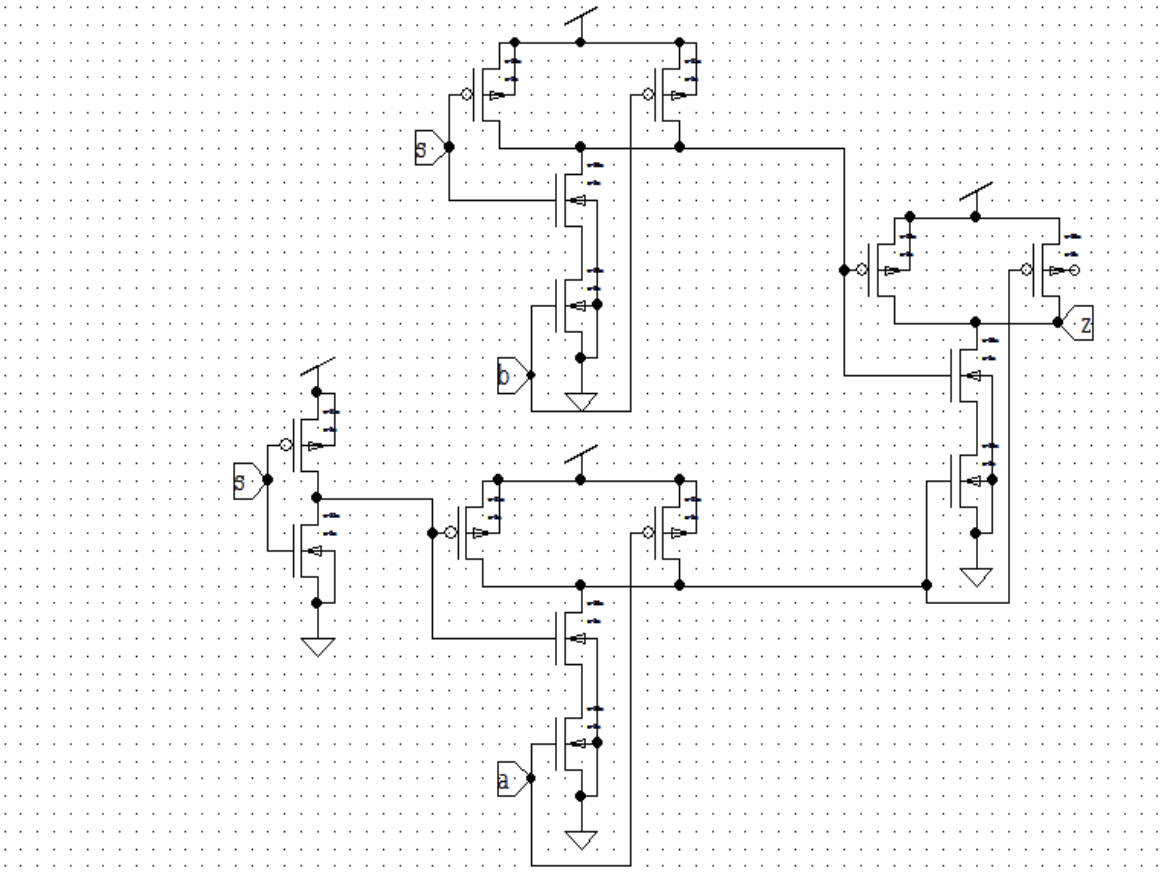

Fig. 3 Schematic of CMOS 2:1 Multiplexer Circuit

The Schematic of CMOS logic based 2:1 multiplexer circuit has shown in the Fig. 3, if both of the A and B inputs are high, then both the NMOS transistors will conduct, neither of the PMOS transistors will conduct, and a conductive path will be established between the output and VSS, bringing the output low. If both of the A and B inputs are low, then neither of the NMOS transistors will conduct, while both of the PMOS transistors will conduct, establishing a conductive path between the output and VDD, bringing the output high. If either of the A or B inputs is low, one of the NMOS transistors will not conduct, one of the PMOS transistors will, and a conductive path will be established between the output and VDD, bringing the output high. As the only configuration of the two inputs that results in a low output is when both are high, this circuit implements a NAND logic gate.

2.4 PSEUDO NMOS Logic Based Multiplexer Circuit

The design of Pseudo NMOS Logic is shown in Fig.4.Using a PMOS transistor simply as a pull-up device for an n-block is called pseudo-NMOS logic. The pull-up transistor must be chosen wide enough to conduct a multiple of the n-block's leakage and narrow enough so that the n-block can still pull down the output safely

The advantage of pseudo-NMOS logic are its high speed (especially, in large-fan-in NOR gates) and low transistor count. On the negative side is the static power consumption of the pull-up transistor as well as the reduced output voltage swing and gain, which makes the gate more susceptible to noise. At a second glance, when pseudo-NMOS logic is combined with static CMOS in time critical signal paths only, the overall speed improvement can be substantial at the cost of only a slight increase of static-power consumption. Furthermore, when the gate of the pull-up transistor is connected to a appropriate control signal it can be turned off, i.e., pseudo-NMOS supports a power-down mode at no extra cost.

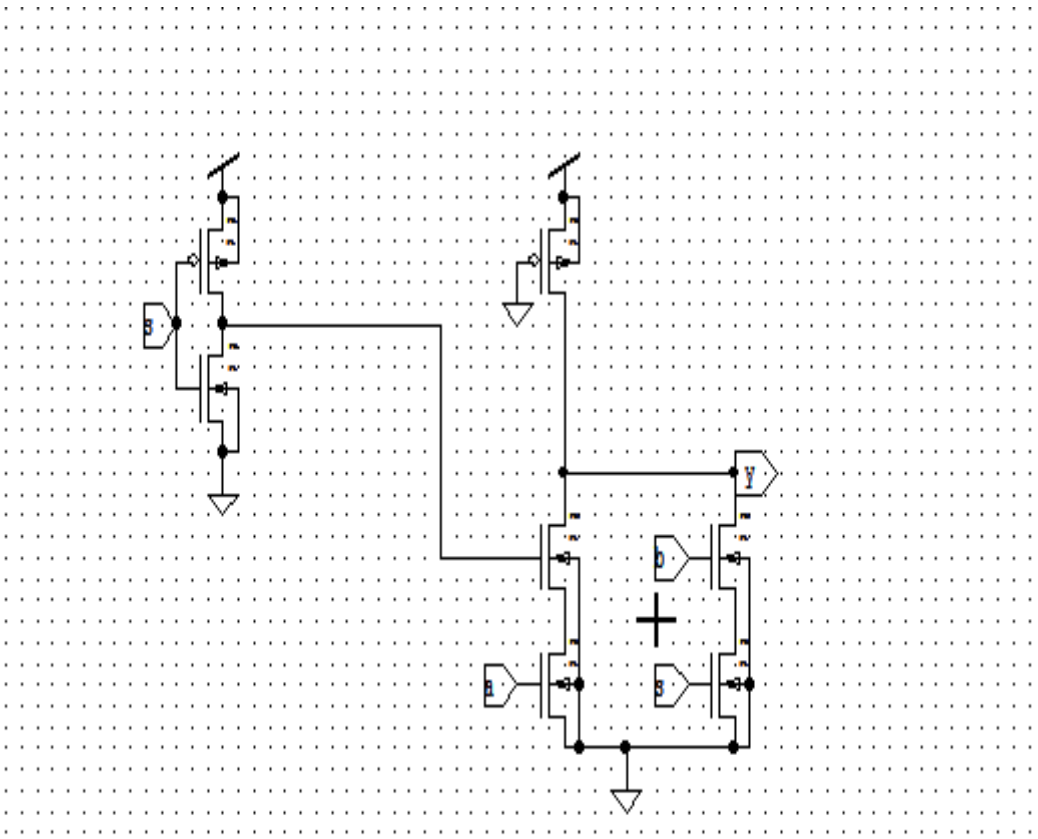

Fig. 4 Schematic of pseudo NMOS logic based 2:1 multiplexer circuit

III. SIMULATION AND ANALYSIS

3.1 Simulation Environment

All the circuits have been simulated using 90 nm technologies on Tanner EDA tool. To make the impartial testing environment all the circuits has been simulated on the same input patterns. Tanner EDA provides of a complete line of software solutions for the design, layout and verification of Analog and Mixed-Signal (A/MS) ICs.T-Spice Pro is Tanner EDA's design entry and simulation system includes S-Edit for schematic capture T-Spice for circuit simulation, and W-Edit for waveform probing.

3.2 Performance Analysis

TABLE 1 depicts the Delay over a range of Power Supply voltages and as it is shown in the table that Pseudo NMOS Logic circuit for 2:1 multiplexer shows minimum Power and Delay.

TABLE 1: Power Delay Product Comparison of different 2:1 Multiplexer Circuits

PARAMETER	VDD (volt)	Existing DCVSL	MODIFIED DCVSL	Pseudo NMOS Logic	CMOS logic
Power consumption (watts)	0.7 0.8	6.493e-001 7.532e-001	3.1764e+001 1.764e+001	3.5345e+000 1.7084e+001	5.746e-001 6.648e-001
Delay	0.7 0.8	1.82ns 2.19ns	1.64ns 1.27ns	1.64ns 1.09ns	1.64ns 1.09ns

The simulation result for Pseudo NMOS Logic is shown in Fig.5,

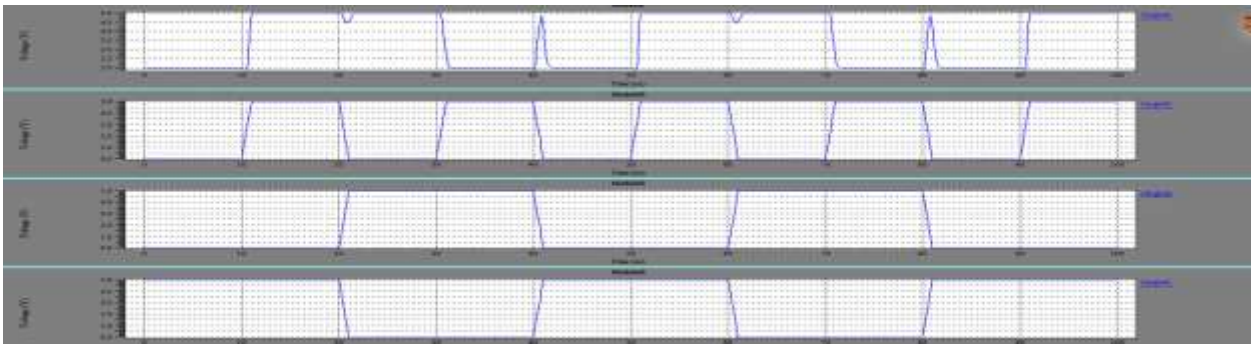

Fig. 4 Simulation result for pseudo NMOS logic based 2:1 multiplexer circuit

IV. CONCLUSION

The post layout simulation have been done for the for pseudo NMOS logic based 2:1 multiplexer circuit in order to show the improvement in power consumption and delay over different supply voltage. The proposed 2:1 multiplexer has been designed and proved it to be a better option for low power complex system design. The net effect is that for pseudo NMOS logic based 2:1 multiplexer circuit shows a much better performance compared to all other 2:1 multiplexer. In future different logic are going to implement to obtain low power consumption and delay.

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