A NOVEL SINGLE-PHASE FIVE-LEVEL INVERTER WITH COUPLED INDUCTORS

Chavala V S Ramanjaneyulu [1], K.V.Gopala Chari [2]

[1]M.Tech Scholar (PE), [2]Professor, Deptt. of EEE

Nalanda Institute of Engg and Tech. (NIET), Siddharth Nagar, Guntur, A.P, (India)

ABSTRACT

This paper deals with, a novel single-phase five-level inverter is implemented by using coupled inductors. This inverter can produce the output of five level voltages with only using one dc source. There is no requirement of split dc voltage for the capacitor, totally neglecting the voltage balancing problem in conventional multilevel inverters. In all conditions the level of the produced output voltage is only 50% of the dc-link voltage, leading to very effective reduction indv/dt. This inverter is designed based on the commonly used three-arm power module device and the voltage problems on all the power electronic switches are the same, designing of the circuit is very easy to construct. Working procedure of this inverter mechanism is examined and the possible switching configurations are considered. Depended on these analyses, a novel improved modulation technique is developed. With this modulation method, no dc component ripples occurred in the inductor currents, which is very supportive for reduction of the inductors. Simulation and experimental results demonstrate the validity of the implemented inverter composed with the improved modulation technique.

Index Terms: Power Converters, Multilevel Converters, Single-Phase, Pulse Width Modulation.

I. INTRODUCTION

Meanwhile their introduction, multilevel inverters have been getting much consideration and as a result many different technologies have been implemented. The academic papers and theses concentrating on multilevel inverter methods are almost countless. These methods can be divided according to many standards. This paper wills emphasis on single-phase high level inverters. For instant single-phase multilevel inverters, the greatest common methods are the cascaded, capacitor clamped, and types diode-clamped. There happened many other implementations. In universal, multilevel inverter methods can be confidential into two types: those are Type I and Type II.

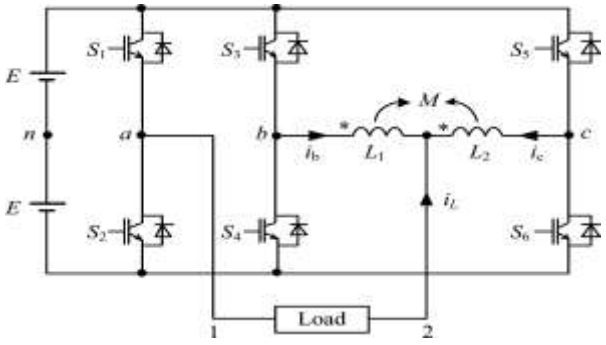

Fig.1. Proposed Single-Phase Five-Level Inverter.

Type I customs multiple dc voltage bases and Type II procedures multiple (split or clamping) dc voltage capacitors. Type I comprise the conventional cascaded techniques, those accessible in and so forth. Type II contains the traditional capacitor-clamped inverters, diode-clamped, the technologies suggested. In terms of single phase multilevel inverters, the drawbacks of the two types are deceptive. Type I drawback from the accessibility of the multiple dc voltage sources required. In preparation, bulky transformers may be of low or medium frequency is usually essential if a Type I inverter is implemented. This is an excessive challenge to when it comes to weight, volume, and cost reduced.

The drawback with Type II is mostly the complementary of the dc capacitor voltages; however some technologies can accomplish self-balancing with confident control algorithms. A multilevel inverter by only one dc source and no requirement of split capacitors may be the most necessary technology but inappropriately this category of inverter has still to be exposed. Freshly multi-level inverters with coupled inductors have strained some investigators 'concentration and a half-bridge three-level inverter has been implemented using two power switches, two diodes, two coupling inductors and weight. Moreover, as goaled at single-phase five-level consists of two such type of half-bridges, overall six power electronic devices necessary (four power switches, two diodes) and four coupled inductors will be required. What is more, dc component consistent happens in the inductor current in these of inverters, which is destructive to the full usage of the attractive cores.

More freshly, accessible single-phase inverter termed as a five-level-active-neutral-point clamped through coupled inductor (5L-ANPC-CI). The 5L-ANPLCIinverter expenditures eight power electronic switches, and divided of the dc-link capacitor is desirable. Thus, the danger of disturbed capacitor voltage occurs if the inverter is not appropriatelymoderated.This paper develops a novel single-phase five-level inverter proposed with coupled inductors and the traditional three-arm power components (see Fig. 1).With the implemented inverter, only one dc voltage source is required and fragmented of the dc voltage capacitor is also negligible, which vanishes the trouble of dc capacitor voltage balancing with the conventional methods.

Temporarily, six power switches with the identical voltage stress and only use one set of coupled inductors are implemented. Also, fewerinductorsare desired inthe inverter developed in this paper associated with the methodology. In accumulation, an enhanced modulation arrangement of this inverter also exists. With this modulation technique, nodc component happened in the inductor currents below all load circumstances, which will advantage the full use of the magnetic cores and reduction of the inductors. Theoretical examines, numerical reproduction, and experimental results are accessible to show the strength of the implemented inverter with the improved modulation technique.

II. OPERATION AND PRINCIPLES

Fig. 1 demonstrations the circuit of the suggested single-phase five level inverter with coupled inductors. In Fig. 1, 2E is the dc-link supply voltage and $L1$ and$L2$ are the two coupled inductors. The mutual inductance of the double inductors is M and the output points of this inverter are1 (the identical point as the output of arm a) and 2. Clearly, this technology is very humble and can be assembled simply by addition of two coupled inductors to a conservative three-arm inverter bridge.

2.1 Role of the Coupled Inductors

It is, in detail, the implementation of the coupled inductors that kinds it conceivable to output five-level voltage by only one dc voltage source. So the part of the coupled inductors will be examined first.

Assume that the two combined inductors are with the equal number of turns or attained through a center-tapped inductor. The self-leakage inductances of the two inductors are $L\sigma 1$ and $L\sigma 2$,correspondingly.Supposing that $L\sigma 1 = L\sigma 2 = L\sigma$, the voltage calculations of the coupled inductors can be stated as given:

$$\frac{(M+L_\sigma)\frac{dIb}{dt}-MdI_c}{dt} = U_{bn} - U_{2n} \ldots(1)$$

$$\frac{(M+L_\sigma)\frac{dIc}{dt}-MdI_b}{dt} = U_{cn} - U_{2n} \ldots(2)$$

Temporarily, giving to Kirchhoff's current law, one can acquired

$$I_b + I_c + I_L = 0 \ldots\ldots\ldots\ldots..(3)$$

From (1) to (3), the subsequent equation can be derivative:

$$U_{2n} = \frac{U_{bn}+U_{cn}+(L_\sigma)\frac{dIL}{dt}}{2} \ldots\ldots\ldots\ldots..(4)$$

Commonly, the leakage inductance can be deliberated to be very small and its effect can be neglected in most circumstances. Consequently, (4) can be altered as

$$U_{2n} = \frac{U_{bn}+U_{cn}}{2} \ldots\ldots\ldots\ldots..(5)$$

This result is fascinating and demonstrations that the coupled inductors will accomplish as an addition of the two input voltage is measured at the non-common-connected stations with the common-connected points as the output. Essentially, deprived of the help of the coupled inductors, the suggested inverter will not be talented to output five-level voltage.

S_1	S_3	S_5	u_{12}
1	0	0	$+2E$
1	0	1	$+E$
1	1	0	$+E$
1	1	1	0
0	0	0	0
0	0	1	$-E$
0	1	0	$-E$
0	1	1	$-2E$

Table I: Switching States and Output Voltage of the Proposed Inverter

2.2 Switching States for Five-Level Output Voltage

From Fig. 1 and (5), the produced output voltage of the implemented inverter can be written as

$$U_{2n} = U_{1n} - U_{2n} = \frac{U_{1n}-(U_{bn}+U_{cn})}{2} \ldots(6)$$

In the following conversation, the power electronic switches in one arm are expected to switch simultaneously. For occurrence, $S2$ necessityistwisted OFF if $S1$ is switched ON and vice versa. So the conversation wills only emphasis on the switching states of $S1$, $S3$, and $S5$. For accessibility of examination, the number "1" will be used to represent the ON condition of one switch and "0" will be used to represent the OFF condition.

In statistic, $u1n$,ubn, and ucn all can produce two-level voltage ($+E$ and $-E$). Rendering to (6), the voltage levels of $u12$ can be given in Table I. Apparently, the suggested inverter can produce five voltage levels at its output points. From Table I, it must be identified out that the switching state of $S1$ should be 1 if $u12 \geq 0$ and the switching state of should be 0 if $u12 \leq 0$.

These incomes*S*1 and *S*2 will conduct at the operated minimum frequency of the reference signal. Consequently, the switching victims of *S*1 and *S*2 will be very lessin the developed inverter.

III. PROPOSED MODULATION METHOD

Even though the suggested inverter can output five-level voltage, the modulation technique must be examined in detail for safe procedure. These sections will attention on the pulse-width modulation (PWM) scheme for this inverter.

From the above examination, the switching condition of *S*1 is concerned by the symbol of *u*12ref *S*1 is 1 if *u*12ref ≥ 0 and *S*1 is 0 if *u*12ref ≤ 0, which is very simple to develop Nonetheless, the switching conditions of *S*3 and *S*5 cannot be designated without suspicious study. To decide the switching conditions of (*S*3, *S*5), the following four stages will be discussed:

Case I:*(+E < u*12ref *<+ 2E):* In this stage, the voltage of *u*12 should substitute between +2*E* and +*E*. Rendering to Table I, the switching conditions of (*S*3 , *S*5) within every operating period *Ts* can be (0, 0)↔(0, 1) (defined as *SS*1 , the note "*x*↔*y*" means changing between *x* and *y*) or (0, 0)↔(1, 0).

(S_3, S_5)	S_1	u_{12}	u_{bc}
(0, 0)↔(0, 1): *defined as* SS_1	1	+2E↔+E (*Case I*)	0↔-2E
	0	0↔-E (*Case III*)	
(0, 0)↔(1, 0): *defined as* SS_2	1	+2E↔+E (*Case I*)	0↔+2E
	0	0↔-E (*Case III*)	
(0, 1)↔(1, 1): *defined as* SS_3	1	+E↔0 (*Case II*)	-2E↔0
	0	-E↔-2E (*Case IV*)	
(1, 0)↔(1, 1): *defined as* SS_4	1	+E↔0 (*Case II*)	+2E↔0
	0	-E↔-2E (*Case IV*)	

Table Ii Switching States Suitable For (*S*3,*S*5)

Case II :*(0 ≤ u*12ref *<+E):* In this occurrence, the voltage of *u*12 must be shift between +*E* and 0. Depended on Table I, the switching stages of (*S*3,*S*5) within every *Ts* can be (0,) ↔ (1, 1) (definite as *SS*3) or (1, 0) ↔ (1, 1) (definite as *SS*4).

Case III: *(−E < u*12ref *≤ 0):* In this situation, the voltage of *u*12wouldchange between +0 and −*E*. Conferring to Table I, the switching conditions of (*S*3 , *S*5) within every *Ts* can be (0,0)↔(0,1) (which is previously definite as *SS*1 in Case I) or (0, 0)↔(1, 0)(which is previously definite as *SS*2 in Case I).

Case I: *(−2E < u*12ref *<− E):* In this occurrence, the voltage of *u*12 would alternate between−*E* and−2*E*. Depended on Table I, the operating stages of (*S*3 , *S*5)within every *Ts* can be (0, 1)↔(1,1) (which is previously definite as *SS*3 in Case II) or (1, 0)↔(1, 1)(which is previously defined as *SS*4 in Case I).

From the above investigation, one can accomplish that only four types of switching conditions within every operating period *Ts* can be designated for (*S*3 , *S*5), i.e., *SS*1 , *SS*2 , *SS*3 , and *SS*4 , which are noticed in Table II. Temporarily, if the reference required voltage *u*12ref is given within convinced, there are continuously two conceivable choices,i.e., Case I and Case III has *SS*1 or *SS*2 for and Case II and Case IV has *SS*3 or *SS*4.

For further conversation, the dwelling time for the operated switch that switches within specified period Tsis definite as

$$T_{D\ well} = \frac{\left(\left|U_{12ref}\right| - K.E\right).T_s}{E} \quad \text{.....(7)}$$

Where the integer *K* is premeditated by

$K=\text{floor}\frac{(|U_{12ref}|)}{E}$…….(8)

The purpose of floor(*x*) rounds *x* to the adjacent integer less than *x*. Clearly, the dwelling time in (7) can be produced by the traditional triangle wave which is exposed in Fig. 2. For accessibility of considerate, the green parts in Fig. 3 demonstrate the dwelling time within every operating period *Ts.*

Essentially, the implemented inverter can be controlled in such a way that only at a time one of *S*3 and *S*5 carries out the dwelling time although the other one is continuously ON or OFF within one specified *Ts* . Taking Case I as an instance, if *SS*1 is designated, *S*5 will switched ON and transmit out the dwelling time even though*S*3 is every time OFF within one conduction period *Ts*; if *SS*2 is nominated, *S*3 will switched ON and carry out the dwelling time while *S*5 is chosen OFF within one *Ts.*

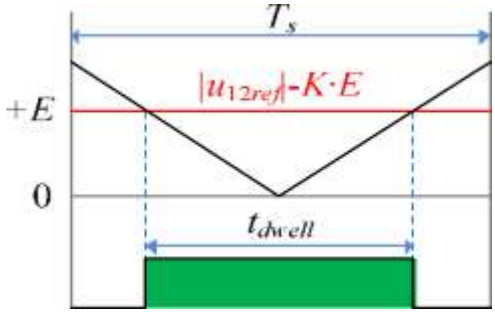

Fig.2. Generation of the Dwelling Time Defined In (7)

As there are constantly two adoptions for selecting the switching conditions of (*S*3, *S*5), a great numerous switching arrangements can be originate within one essential period. Fig.3 just demonstrations six of the promising switching designs for (*S*3,*S*5), i.e., *SP*1–*SP*6. All of these switching arrangements can produce the five-level output voltage *u*12 as exposed in Fig. 3. Conversely, as the coupled inductors are associated between arms *b* and *c*, the voltage *ubc* may comprise dc or important components in case of inadequate modulation.

If dc component happens in *ubc*, the currents flowing in the coupled inductors may raise to quite a huge value, which is very risky to the standard working performance of the inverter. In order to work the inverter securely and reduce the weight and size of the coupled inductors, the resulting rules for modulation must be satisfied.

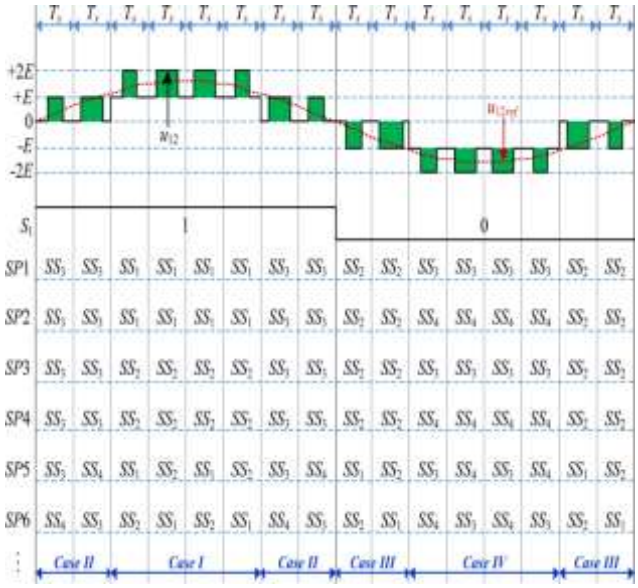

Fig.3. Dwelling time (green part) within every *Ts* and the some of the possible switching patterns for *S*3 and *S*5 (*SP*1–*SP*6)

1) The voltage *ubc* must not comprise any dc component. Then, the inverter may have the danger of high current.

2) The currents in the coupled inductors may not be containing slightly fundamental or low order harmonic constituent under no-load situation. Else, the magnetization current and the core of the inductors current composed with the inverter losses will be improved, leading to reduced effectiveness and reliability of the inverter and increased flux density of the inductor core.

Considering the above instructions, not all of the conceivable switching designs for (*S*3,*S*5) can be designated. Certainly, the two possible selections (for Case I and Case III has *SS*1 or *SS*2 and for Case II and Case IV*SS*3 or *SS*4) for (*S*3,*S*5)inside one *Ts* have the similar part on the output voltage, but the voltage *ubc* they produce differs a lot. For example, it is realized from Table II that both*SS*1 and *SS*2 can produce an desired output voltage changes between+2*E* and +*E* (0 and −*E*) if the operating state of *S*1 is 1 (0).

Specifically, *SS*1 and *SS*2 have the same part on the desired output voltage of this inverter. While, if *SS*1 is assumed, the voltage at coupled inductors *ubc* will be 0 or −2*E* although*ubc* will be 0 or+2*E* if *SS*2 is recognized. If *SS*1 creates the current in the coupled inductors escalated, *SS*2 will create that current reduction and vice versa. This is also correct for *SS*3 and *SS*4.

Consequently, *SS*1–*SS*4cannot be designated in successive switching periods without alteration. Then, fundamental or low-order ripples will presented in the inductor currents below no load and it will also raise the inductor currents while the inverter is loaded. Depended on these evaluations, the proper modulation or switching approach for the implemented inverter can be attained.

The possible switching states for (S_5, S_6) in the $(k\text{-}1)^{th}$ T_s	The possible switching states for (S_5, S_6) in the k^{th} T_s
SS_1	SS_2 for *Case I* and *III*
	SS_4 for *Case II* and *IV*
SS_2	SS_1 for *Case I* and *III*
	SS_3 for *Case II* and *IV*
SS_3	SS_2 for *Case I* and *III*
	SS_4 for *Case I* and *IV*
SS_4	SS_1 for *Case I* and *III*
	SS_3 for *Case II* and *IV*

Table Iii Rules for Selecting Switching States of (*S*3,*S*5)

Switching designs shown in Fig. 3 are not all appropriate. For instance, *SP*1–*SP*4 does not meet the instructions listed in Table III while *SP*5 and *SP*6 are proper.

IV. CONCLUSION

This paper suggested a novel single-phase five-level inverter by using the coupled inductors. This inverter can produce output five-level voltage by only using one dc source and no fragmented of the dc voltage capacitor requirements, totally vanishing the voltage balancing troubles. The height of the stairway in the produced output voltage is only 50% of the dc-link voltage below any inflection index. Temporarily, the voltage stresses or voltage harmonics on all the power electronic switches are the similar and only four switches are functioned at large frequency.

Operation techniqueof this inverter was examined and the enhanced switching arrangements were also accessible to decrease the passive constituent. Verification results show strength of the suggested technology together with the modulation technique. The coupled inductors might be the defect of this converter. Conversely, the switches charming the high current have low-operating frequency although the switches compelling the low current have high-operating frequency. So, the accessible technology is very appropriate for low to medium power requests, particularly for high-current circumstances.

REFERENCES

[1] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A Surveyof topologies, controls, and applications," IEEE Trans. Ind. Electron.,vol. 49, no. 4, pp. 724–738, Aug. 2002.

[2] M.Malinowski, K. Gopakumar, J. Rodriguez, andM. A. Perez, "A surveyon cascaded multilevel inverters," IEEE Trans. Ind. Electron., vol. 57,no. 7, pp. 2197–2206, Jul. 2010.

[3] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey onneutral-point-clamped inverters," IEEE Trans. Ind. Electron., vol. 57,no. 7, pp. 2219–2230, Jul. 2010.

[4] Y.-S. Lai and F.-S. Shyu, "Topology for hybrid multilevel inverter," IEEProc. Electron. Power Appl., vol. 149, no. 6, pp. 449–458, Nov. 2002.

[5] Y. Hinago and H. Koizumi, "A single-phase multilevel inverter usingswitched series/parallel DC voltage sources," IEEE Trans. Ind. Electron.,vol. 57, no. 8, pp. 2643–2650, Aug. 2010.

[6] H. Akagi and R. Kitada, "Control and design of a modular multilevel cascadeBTB system using bidirectional isolated DC/DC converters," IEEETrans. Power Electron., vol. 26, no. 9, pp. 2457–2464, Sep. 2011.

[7] Y.-H. Liao and C.-M. Lai, "Newly-constructed simplified single-phasemultistring multilevel inverter topology for distributed energy resources,"IEEE Trans. Power Electron., vol. 26, no. 9, pp. 2386–2392, Sep.2011.

[8] J. Shi,W. Gou, H. Yuan, T. Zhao, and A. Q. Huang, "Research on voltageand power balance control for cascaded modular solid-state transformer,"IEEE Trans. Power Electron., vol. 26, no. 4, pp. 1154–1166, Apr. 2011.

[9] F. Z. Peng, "A generalized multilevel inverter topology with self voltagebalancing," IEEE Trans. Ind. Appl., vol. 37, no. 2, pp. 611–618, Jul. 2001.

[10] Y. Ounejjar and K. Al-Haddad, "A novel high energetic efficiency multileveltopology with reduced impact on supply network,," in Proc. IEEE34th Ann. Conf. Ind. Electron. (IECON), 2008, pp. 489–494.

AUTHOR DETAILS

	**Chavala v s ramanjaneyulu,**pursuing M.Tech (PE) Nalanda Institute of Engineering and Technology (NIET),Siddharth Nagar, Kantepudi(V), Satenepalli(M),Guntur Dist., A.P., India
	**K.V.Gopala Chari**, working as aProfessor (EEE) at Nalanda Institute of Engineering and Technology (NIET),Siddharth Nagar, Kantepudi(V), Satenepalli(M),Guntur Dist., A.P., India