AN IMPROVED BUCK PFC CONVERTER WITH HIGH POWER FACTOR

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ABSTRACT

In this paperan improved buck power factor correction (PFC) converter technology is implemented. By providing extra parameters like an auxiliary switch and two diodes, in the conventional buck PFC converter the dead zones in ac input current of can be vanished. An improved fixed ON-time control is implemented and employed in this proposed buck PFC converter to force it that works in critical conduction mode (CRM) of operation.With finestproper regulating parameters, approximately unity power factor can be attained and the harmonics of the input current can meet the IEC61000-3-2 class C standard within the worldwide input voltage assortment. Furthermore, the reliability of the designed converter is not declined compared to the traditional buck converter. Detailed theoretical research, analysis and optimal design deliberations for the implemented converter are accessible and tested by a 100-W lab made prototype.

Keyterms: Buck Power Factor Correction (PFC), AC–DC,Class C, High Power Factor (PF), High Efficiency.

I. INTRODUCTION

Nowa day, maximum ac/dc power converters are required to adequate the harmonic current to meet the desired IEC61000-3-2 limits. Some different power products such as lighting equipment parametersmust maintain the stricter IEC61000-3-2 class C requirements. Power factor correction (PFC) is a efficienttechnique for generating an almost input current is sinusoidal. The boost converter is the effective popular technology for PFC applications because of its essentialcurrent shaping capability. Nonetheless, with common input, generally a 400 Vdc output voltage is essential for the boost PFC. The boost PFC cannot accomplish high productivity at low line input due to it works with huge duty cycle in order to maintain high-voltage conversion gain improvement. Therefore, it is hard to enhance the power density of boost PFC converter because of the thermal distress at low line input. The quadratic buck-boostand Sepic converter can accomplish high power factor (PF) and minimize the output voltage stress. However the voltage ripplesof switch in these two methods is much more than that in the boost PFC converter that diminishes the competence and raises the cost.

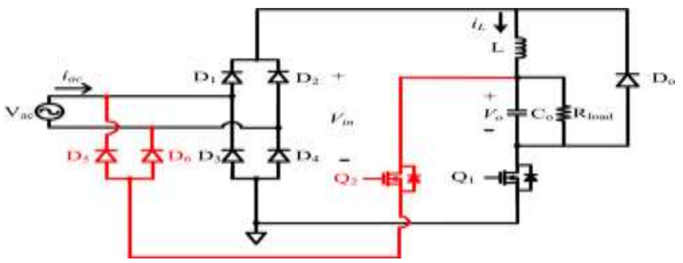

Fig.1. Proposed Improved Buck PFC Converter

The buck PFC converter has some great benefits. First, the desired output voltage of buck converter is regulatedalways lesser than the boost converter. Second, the voltage across the main power electronic switch of the buck converter is nearlycompressed to the input voltage. Consequently, the buck PFC converter can accomplish relatively high reliability within the common\specified given input voltage range and it has produced more and more consideration in the past years.

Conversely, if the buck converter works in hard switching approach, the switching loss particularly at high input will be huge, which declines the quality of the buck converter? The buck dc– dc converter functioning in critical continuous conduction mode (CRM) can diminish the reverse recovery problems in diode and succeed zero voltage switching (ZVS) for the major device switch.

The fixed ON-time (COT) regulation for CRM buck PFC converter is presented, Through COT control, the peak current in the switch is nearlydirectly proportional to the input voltage, and then high Power Factor can be generated. Conversely, it is still problematic to pass the IEC61000-3-2 situation because of the dead zones in the input current that presents when the input voltage is smaller than desired output *VO*. This developedCOT control can help increase the PF of the traditional buck PFC converter. But, this improved COT control technique needs careful parameters with proper design. Even so, it is still difficultto maintain the limits forced to IEC61000-3-2 class C Standards at the low line supply voltage.

Actually this paper, an advanced buck PFC converter is implemented, as displayed in Fig. 1. Associated with the traditional buck PFC converter, asupplementary switch and two diodes are additionalto the improved buck PFC converter. The suggested converter has two distinct modes of operations in a line period. When the input voltage is larger than the desired output voltage, the implemented converter works in buck mode, which is identical as the traditional buck converter. When the supply voltage is smaller than the required output voltage, the implemented converter works in buck-boost mode.

Therefore, there are no dead zones in the supplied input current. The PF can be enhancedvisibly, and then the designed converter can maintain IEC61000-3-2 class C standards simply with sufficientmargins Furthermore, the reliability of the suggested converter is very adjacent to the traditional buck converter. The presented converter is appropriate for the PFC front side of ac/dc converter and the power range from 60 to 300 W is maintained by LED drivers with.

II. PRINCIPLE OF OPERATION

In this section, the suggested converter works in CRM will be examined in detail. To abridge the analysis, the evolutions between the switches and the output diode *Do*are neglected. After that, there still happened eight modes operationin a line period.

2.1 Positive Buck-Boost Operation Mode

When the supplied input voltage *V*ac is in positive half cycle and the amplitude of *V*ac is lower than *VO*, the presented converterworks in buck-boost stage. In this mode, switch *Q*1keeps switched OFF and switch*Q*2 keeps switching ON. There are two modeswhen the developed converter functioning under this mode.

Stage1: When switch *Q*2 is switched ON, the suggested converter works in stage 1. The corresponding circuit of this stage is exposed in Fig. 2(a). During this mode of operation the inductor *L* is Store energy by *V*ac through *D*1 and *D*6, and current *IL* increases.

Stage 2: When switch *Q*2 is trigger OFF, the presented converter performs in stage 2. The relevant circuit of this stage is given in Fig. 2(b). During this mode of operation the inductor *L* is released the energy by *VO* through *Do*, and current *IL* decreases.

2.2 Positive Buck Operation Mode

In positive half cyclethe supplied input voltage *V*ac amplitude is larger than desired output *VO*, the implemented converter works in buck mode. During this mode, switch *Q*2 maintains OFF condition and switch *Q*1 maintains ON switching. There are two modes of operation for the designed converter under this situation.

Stage 3: When switch *Q*1 is triggered ON, the suggested converter activates and works in stage 3. The corresponding circuit of this mode arrangement is drawn in Fig. 2(c). During this stage the inductor *L* is situated to charge by *V*ac−*Vo* through *D*1 and *D*4, and current *IL* increases.

Stage 4: When switch *Q*1 is turns OFF, the proposed converter working in stage 4. The relevant circuit of this stage is similar as that of stage 2, as given in Fig. 2(b). During this mode of operation the inductor *L* is releases the stored energy by *VO* through *Do*, and current *IL* decreases.

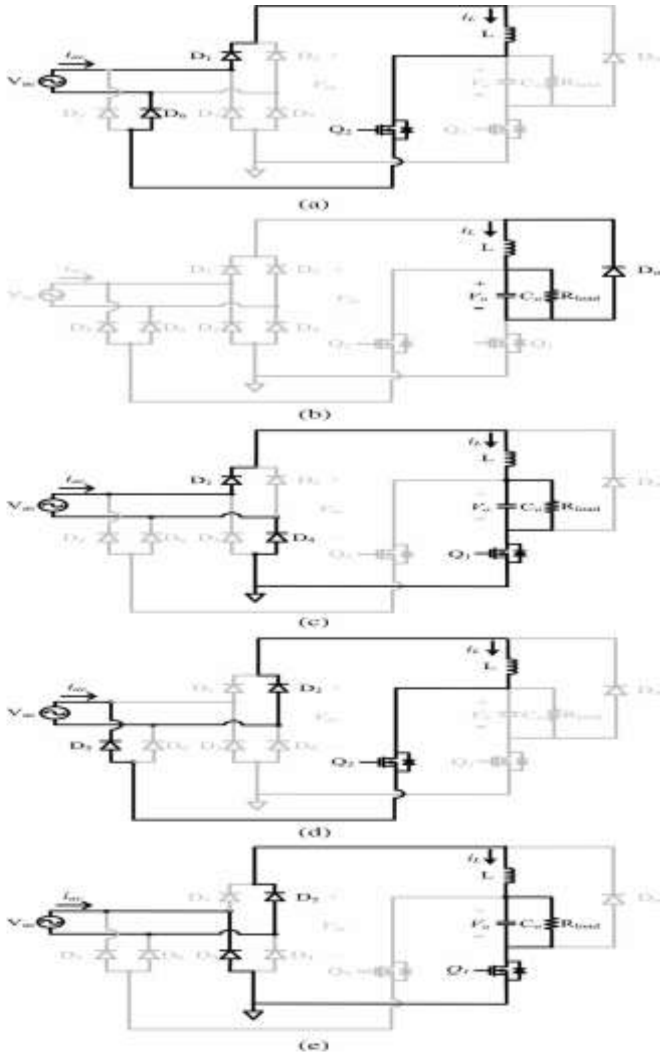

Fig.2. Equivalent Circuits of the Proposed Converter in Eight Stages

When the supplied input voltage *V*ac is goes to negative half cycle region, therealso performs two modes operation of negative buck operation mode and buck-boost operation mode of the developedconverter.

The negative operation procedures can also be situatedinto four operation stages called as stages 5–8, and the corresponding circuits may comprises in Fig. 2(b), (d), and (e). The negative half cycle working processes of the advanced control strategy converter are similar to the positive half cycle operation. For our convenience, the negative mode of operation processes is not illustrated in detail here.

An effectiveCOT control is employed for the regulated controlledbuck PFC converter to force it that must be operates in CRM, as displayed inFig. 3. The desired output voltage is identified with a level-shift circuitdesigned by the resistors *Ra*1 ~*Ra*4 and a high-voltage transistor *Q*2.

The given Fig. 3, the control signal *V*ph is used to regulate theconverter either in buck-boost mode or buck-mode is accomplished bycomparing the recognized*V*IN signal V_{IN} *in* with a desired voltage reference*V*boundary. Generally, *V*boundary is adjusted to sense the output voltage*VO*with the equal ratio as that V_{IN}in modulated*V*IN. *V*ph is high when V_{IN}in is larger than *V* boundary and is low when V_{IN}in is smaller than *V* boundary.

The measured output signal *V*FB is gives to the signal of negative input to the error amplifier *Uf*. The error concerning*V*FB and the desired reference *V*ref is augmented by the compensations network parameters*Cf*and adesired error signal *V*comp is reached.

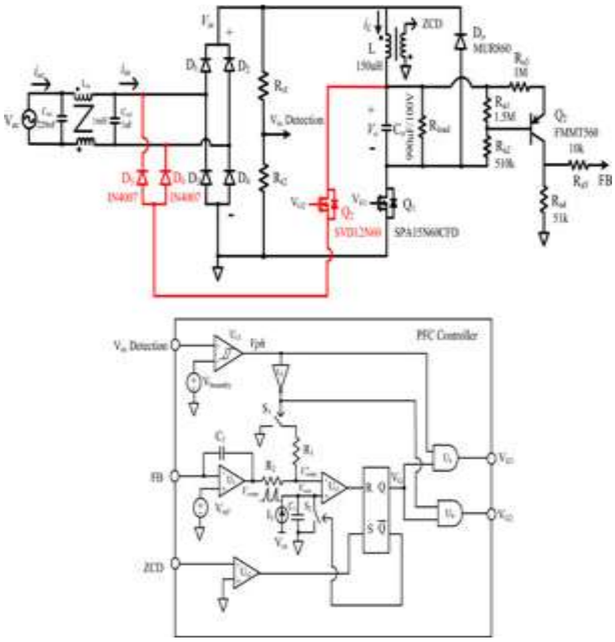

Fig.3. Schematic of the Proposed Buck PFC Converter with an Improved COT Control

The dc voltage signal V_{IN}comp employed to control the conductionperiod i.e. operating period*T*ON is accomplished from *V*compfrom a control networks. It isdesigned by switch *S*1 and resistors *R*1 and *R*2. Switch *S*1 isregulated by the control signal *V*ph. The suggested converterworks in buck mode when *S*1 is triggered OFF and works in buckboostmode when S1 is activated ON.

V_{IN}comp is a step function regulatedby *V*ph, as shown in (1).

$$V'_{comp} = \begin{cases} V_{comp} \ , V_{in} > V_o \\ K.V_{comp} \ , V_{in} \leq V_o \end{cases} \quad .(1)$$

Where*k* specifies the coefficient equal to *R*1 / (*R*1+*R*2). Similar to thetraditional COT control, a fixed current source *I*1, switch *S*2 and capacitor *C*1, are used to produce a saw tooth waveform*V*saw. When *V*sawachievedV_{IN}comp, the comparator output *Uc*1 is stepped from low level to high level. This level conversion resetsthe modulating signal from high level to low level region.

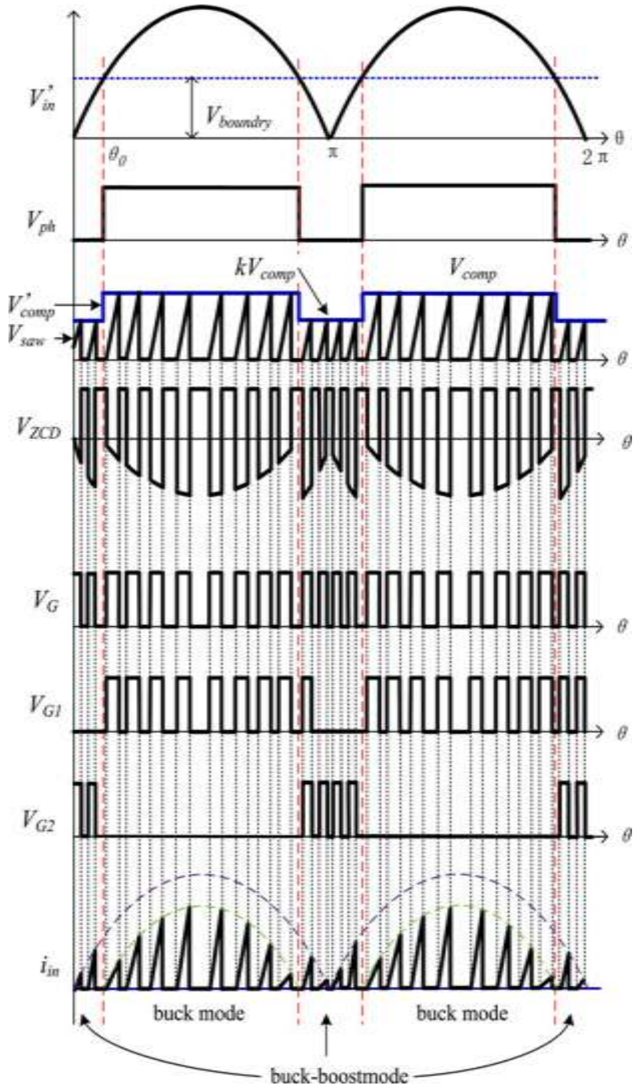

Fig.4. Key Waveforms in the Improved COT Control Diagram

The zero-crossing limit of the inductor current *IL*is distinguishedby the auxiliary winding from inductor *L*. This inductorcurrentzero-crossing detection technique signal *V*ZCD can be employed in both buckand buck-boost stages. When the inductor current *IL*reaches tozero, the auxiliary winding *V*ZCD output voltage starts to decreasing and reaches to zero.Once *V*ZCD falls to zero position, the output of comparator *Uc*2 steppedfrom low level to high level value. This level evolution sets the modulating Signal from low level to high level.

According to the abovementioned explanation, the rising slope of*V*saw is persistentowing to the fixed current source *I*1 accusingduring the entire line period. Consequently, the ON-time (*T*ON) ofthe switches is identified by V_{IN}comp correspondingly. Smallervalue of *k* indications to smaller *T*ON and smaller peak values of current*IL* when the implemented converter is working in buck-boost stage.

As displayed in Figs. 3 and 4, the modulating signals *VG*1 and *VG*2 areregulated by *V*ph for the different operation modes consecutively.

III. CONCLUSION

The improved buck PFC converter technologyimplemented in this paper is simple to accomplish as the construction of the topology is simple. To work in CRM, an advanced and improved COT control is presented. Nearly unit PF can be attained and the input current ripples can meet the IEC61000-3-2 class C standard within the common input voltage range, whereas the reliability is not declined compared to the traditional buck converter.

The main drawback of this suggested topology is that two diodes and a switch are mandatory and the additional switch requires a floating driving point circuit. Conversely, the cost and size enhanced little compared to the complete cost and size.

Detailed theoretical investigation and design attentions of this proposed converter have been accessible and the theoretical examines are proved by a 100-W experimental prototype. Finally, this developed converter is very appropriatefor industrial applications.

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