RELIABILITY IMPROVEMENT IN ZERO BYPASS MULTIPLIER

[1]M. Arunmozhi Devi, [2]S.Srinidhi

[1] PG Scholar, [2]Assistant Professor, Department of VLSI Design,
Theni Kammavar Sangam College of Technology (India)

ABSTRACT

Digital multipliers are among the most critical arithmetic function all units. The overall performance of these systems depends on the through put of the multiplier. Mean while, the negative bias temperature instability effect occurs when a p MOS transistor is under negative bias ($V_{gs} = -V_{dd}$), increasing the there should voltage of the p MOS transistor, and reducing multiplier speed. A similar phenomenon, positive bias temperature in stability, occurs when an MOS transistor is under positive bias. Both effects degrade transistor speed, and in the long term, the system may fail due to timing violations. Therefore, it is important to design reliable high-performance multipliers. In this paper, we propose an aging-aw are multiplier design with a novel adaptive hold logic (AHL) circuit. The multiplier is able to provide higher through put through the variable latency and can adjust the AHL circuit to mitigate performance degradation that is due to the aging effect. Moreover, the proposed architecture can be applied to a column-or row-bypassing multiplier.

Keywords: AHL, NBTI, PBTI.

I.INTRODUCTION

Digital multipliers are among the most critical arithmetic functional units inmanyapplications, such as the Fourier transform, discrete cosine transforms, and digital filtering. The through put of these applications depend son multipliers, and if the multipliers are too slow, he performance of entire circuits will be reduced. Furthermore, negative bias temperature in stability (NBTI) occurs when a pMOS transistor is under negative bias ($V_{gs}= -V_{dd}$). In this situation, the interaction between inversion layer hole sand hydrogen passivated Si atoms breaks the Si–H bond generated during the oxidation process, generating H or H_2 molecules [20].When these molecules diffuse away, interface traps are left. The accumulated interface traps between silicon and the gate oxide interface result in increased threshold voltage (V_{th}), reducing the circuit switching speed. When the biased voltage is removed, the reverse reaction occurs, reducing he NBTI effect .However, there verse reaction does not eliminate all the interface traps generated during the stress phase, and V_{th} is increased in the long term. Hence it is important to design are liable high performance multiplier.

A faster way to implement multiplication is to resort to an approach similar to manually computing a multiplication. The entire partial product are generated at the same time and organized in an array. A multi operand addition is applied to compute the final product. The approach is illustrated in the Fig.1. This set of

operation an be mapped directly in to hardware. There structure is called an array multiplier and combines the following three functions: partial- product generation, partial-product accumulation and final addition.

Four important types of multipliers are available. 1. Array, 2.Baughwooley 3.Braun 4. Wallace tree are constructed using different types of adder cells presented. Then find out the best one in the performance characteristics like power dissipation, speed and area.

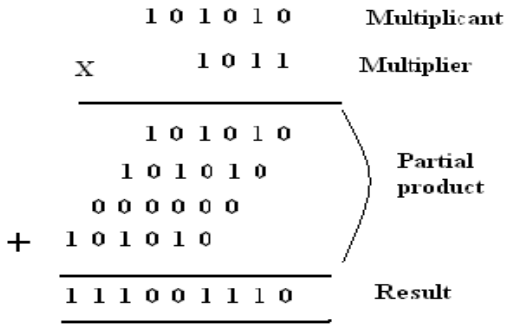

Fig.1. Example of manual multiplication

II. NBTI AND PBTI

Negative Bias Temperature Instability (NBTI) and Positive Bias Temperature Instability (PBTI) are the two well-known circuit reliability issues in these conductor devices. The NBTI in PMOS transistors and the PBTI in the NMOS transistors occur when the transistors are biased in the strong inversion region. The NBTI and PBTI stresses cause the threshold voltage (V_{th}) of transistors drift strongly depending on the stress time and stress condition. This degrade the transistor performance over time. NBTI has been dominant in the poly-gate CMOS technologies. However, both NBTI and PBTI become significant in the high-k metal gate process.

Negative bias temperature instability (NBTI) occurs when a pMOS transistor is under negative bias ($V_{gs}= -V_{dd}$). In this situation, the interaction between inversion layer holes and hydrogen-passivated Si atoms breaks the Si–H bond generated during the oxidation process, generating H or H_2 molecules. When these molecules diffuse away, interface traps are left. The accumulated interface traps between silicon and the gate oxide interface result in increased threshold voltage(V_{th}), reducing the circuit switching speed. When the biased voltage is removed, the reverse reaction occurs, reducing the NBTI effect.

However, the reverse reaction does not eliminate all the interface traps generated during the stress phase, and V_{th} is increased in the long term. Hence it is important to design a reliable high performance multiplier. The corresponding effect on an nMOS transistor is positive bias temperature instability (PBTI), which occurs when an nMOS transistor is under positive bias.

III.BACKGROUND AND RELATED WORK

These are the modules used to achieve reliable high performance multiplier even after aging occur. These are the modules in aging aware reliable high performance multiplier.

1. Array Multiplier

2. Column Bypass Multiplier

3. Row Bypass Multiplier

4. Razor flip-flop

5. AHL Circuit

3.1. Array Multiplier

A multiplier is one of the key hardware blocks in most digital and high performance systems such as FIR filters, digital signal processors and microprocessors etc. Many researchers have tried and are trying to design multipliers which offer either of the following high speed, low power consumption, regularity of layout and hence less area or even combination of them in multiplier. Thus making them suitable for various high speed, low power, and compact VLSI implementations. Generally as all we know multiplication goes in two basic steps.

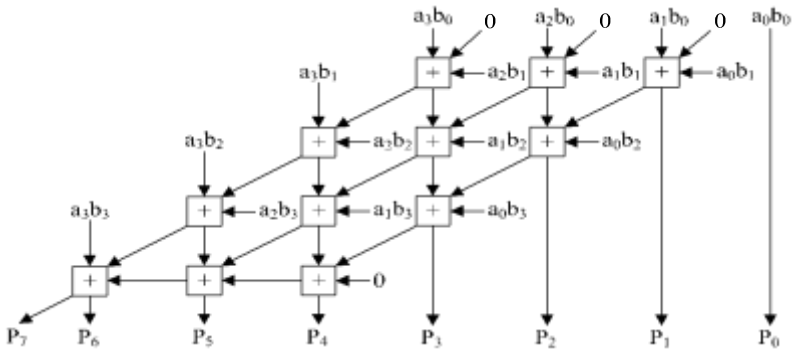

Fig.2.4×4 Array Multiplier

3.2. Column Bypass Multiplier

A column bypassing multiplier is an improvement on the normal array multiplier (AM).The AM is a fast parallel AM and is shown in Fig.2. The multiplier array consists of (n−1) row carry save adder (CSA), in which each row contains (n−1) full adder (FA) cells. Each FA in the CSA array has two outputs:

1) The sum bit goes down 2) The carry bit goes to the lower left FA. The FA in the AM are always active regardless of input states. In a low-power column-bypassing multiplier design is proposed in which the FA operations are disabled if the corresponding bit in the multiplicand is 0. Fig.3 shows a 4×4 column-bypassing multiplier. Suppose the inputs are 1010_2*1111_2, it can be seen that for the FA in the first and third diagonals, two of the three input bits are 0: the carry bit from its upper right FA and the partial product a_ib_i. Therefore, the output of the adders in both diagonals is 0, and the output sum bit is simply equal to the third bit, which is the sum output of its upper FA.

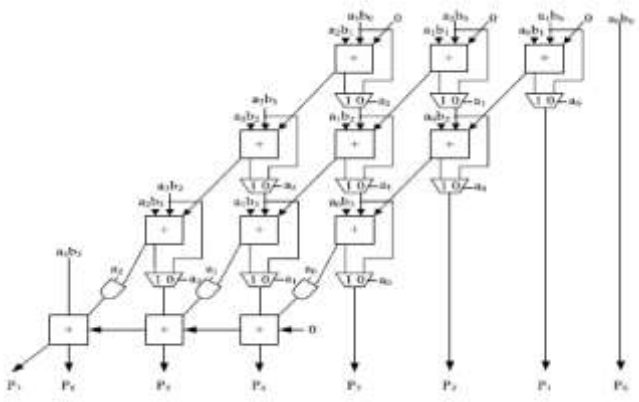

Fig.3. 4×4 Column Bypassing Multiplier.

3.3. Row bypass multiplier

A low-power row-bypassing multiplier is also proposed to reduce the activity power of the AM. Fig.4 is a 4×4 row-bypassing multiplier. Each input is connected to an FA through a tri-state gate. When the inputs are 1111_2 *1001_2, the two inputs in the first and second rows are 0 for FAs. Because b_1 is 0, the multiplexers in the first row select a_ib_0 as the sum bit and select 0 as the carry bit. The inputs are bypassed to FA in the second rows, and the tri-state gates turn off the input paths to the FAs. Therefore, no switching activities occur in the first-row FAs; in return, power consumption is reduced. Similarly, because b_2 is 0, no switching activities will occur in the second-row FAs. However, the FAs must be active in the third row because the b_3 is not zero.

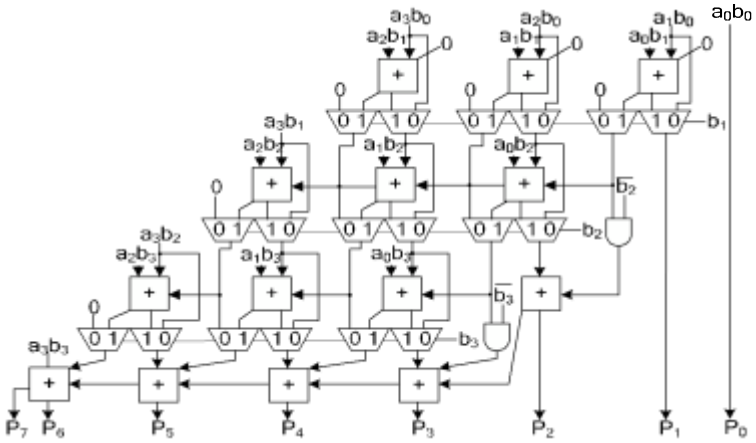

Fig.4. 4×4 Row Bypassing Multiplier.

3.4. Razor Flip-Flop

Razor relies on a combination of architectural and circuit level techniques for efficient error detection and correction of delay path failures. The concept of razor is illustrated in Figure for a pipeline stage. Each flip-flop in the design is augmented with a so called shadow latch which is controlled by a delayed clock. And illustrate the operation of razor flip-flop in Fig. 5. In clock cycle1, the combinational logic $L1$ meets the setup time by the

rising edge of the clock and both the main flip-flop and the shadow latch will latch the correct data. In this case, the error signal at the output of the XOR gate remains low and the operation of the pipeline is unaltered.

To guarantee that the shadow latch will always latch the input data correctly, the allowable operating voltage is constrained at design time such that under worst-case conditions, the logic delay does not exceed the setup time of the shadow latch [9]. By comparing the valid data of the shadow latch with the data in the main flip-flop, an error signal is then generated in cycle 3 and in the subsequent cycle, cycle 4, the valid data in the shadow latch is restored into the main flip-flop and becomes available to the next pipeline stage *L*2.

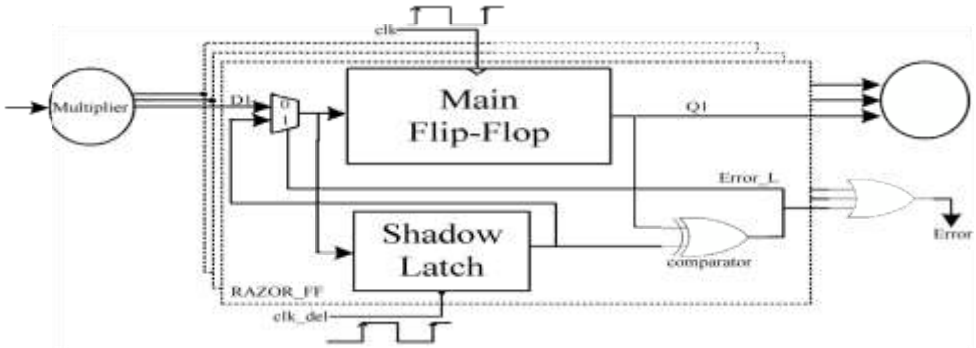

Fig .5. Razor flip-flop structure

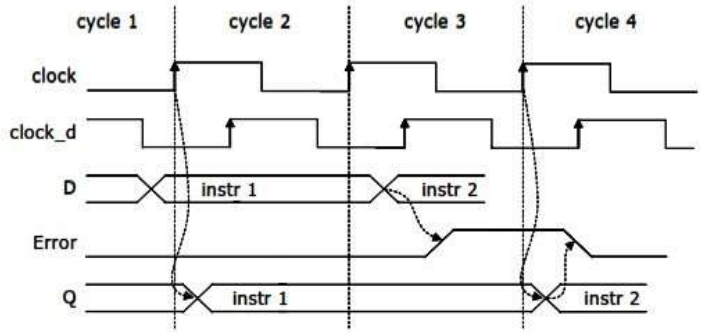

Fig. 6. Operation of Razor Flip-flop

3.5. Ahl Circuit

The AHL circuit is the key component in the aging-ware variable-latency multiplier. Fig. 7 shows the details of the AHL circuit. The AHL circuit contains an aging indicator, two judging blocks, one mux, and one D flip-flop. The aging indicator indicates whether the circuit has suffered significant performance degradation due to the aging effect. The aging indicator is implemented in a simple counter that counts the number of errors.

These timing violations will be caught by the Razor flip-flops, which generate error signals. If errors happen frequently and exceed a pre-defined threshold, it means the circuit has suffered significant timing degradation due to the aging effect, and the aging indicator will output signal 1; otherwise, it will output 0 to indicate the aging effect is still not significant, and no actions are needed.

The first judging block in the AHL circuit will output 1 if the number of zeros in the multiplicand (mr for the RBPM) is larger than *n*. If the number of zeros in the md (mr) is larger than *n*+1. They are both employed to decide whether an input pattern requires one or two cycles, but only one of them will be chosen at a time. In the beginning, the aging effect is not significant, and the aging indicator produces 0, so the first judging block is used. After a period of time when the aging effect becomes significant the second judging block is chosen. Compared with the first judging block, these judging block allows a smaller number of patterns to become one-cycle patterns because it requires more zeros in the multiplicand (mr).

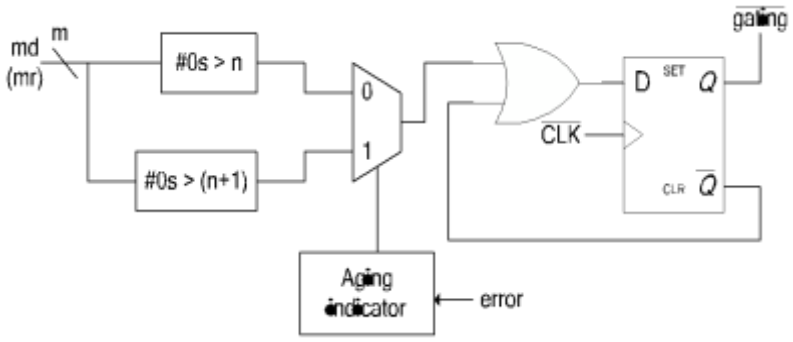

Fig. 7.AHL circuit

IV.PROPOSED METHOD

Aging Aware Reliable Multiplier's Operation

When input patterns arrive, the CBPM or RBPM, and the AHL circuit execute simultaneously. According to the number of 0's in the md (mr), the AHL circuit decides if the input patterns require 1 or 2 cycles. If the input pattern requires two cycles to complete, AHL will output 0 to disable the clock signal of the flip-flops. Otherwise, AHL will output 1 for normal operations. When the column or row bypassing multiplier finishes the operation, the result will be passed to the Razor flop-flop.

If timing violations occur, it means the cycle period is not long enough for the current operation to complete and that the execution result of the multiplier is in correct. Thus, the Razor flip-flops will output an error to inform the system that the current operation needs to be re-executed using two cycles to ensure the operation is correct. In this situation, the extra re-execution cycles caused by timing violation incurs to overall average latency. However, our proposed AHL circuit can accurately predict whether the input patterns require one or two cycles in most cases. Only a few input patterns may cause a timing variation when the AHL circuit judges incorrectly.

In summary, our proposed multiplier design has some key features. First, it is a variable latency design that minimizes the timing waste of the non critical paths. Second, it can provide reliable operations even after the aging effect occurs. The Razor flip-flops detect the timing violations and re-execute the operations using two cycles. When the circuit is aged, and many errors occur, the AHL circuit uses these judging block to decide if an input is one cycle or two cycles.

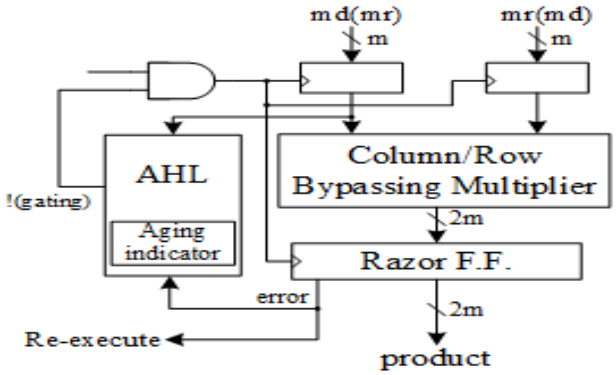

Fig. 8. Aging Aware Reliable Multiplier with AHL

V.SIMULATIONS AND RESULTS

A simulation result for Array Multiplier, CBPM, RBPM is simulated in a Xilinx ISE 9.2 and QUARTUS II 9.1 Web Edition. These tools will help to analyze its performance and calculate the power, delay (τ), total thermal power dissipation and core dynamic thermal power dissipation for all three.

For Reset = 1; Clk = 1; The error will be occur as the difference in data1 and data2 with respect to the normal and delayed clock for both md and mr bit. For the combination of 9*9 the output is 81 but here we obtain the result as 67 but after two clock pulse we get the actual value as 81 for a same input combination. This is shown in Fig. 9. Aging aware multiplier with missing data.

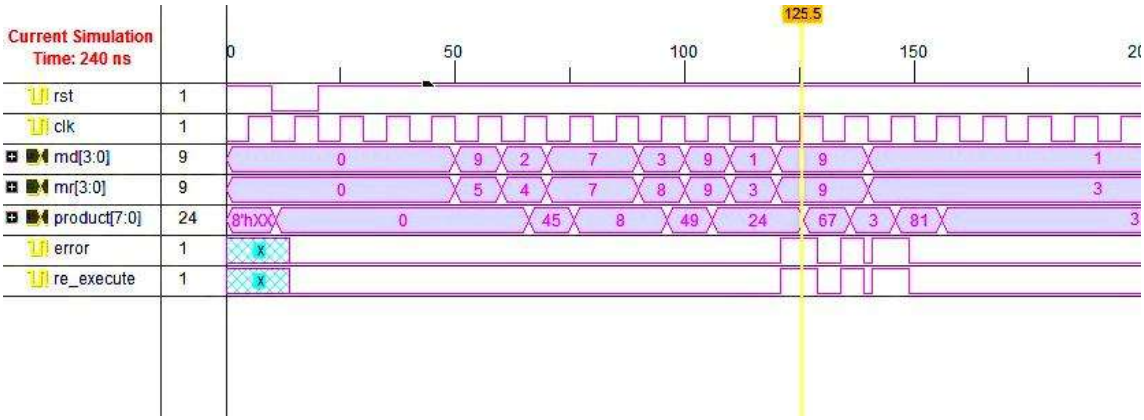

Fig. 9. Aging aware multiplier with missing data

The no of zeores in both multiplicand and multiplicator is calculated by using Xilinx as shown in Fig.10. No of zeroes for corresponding md bit.

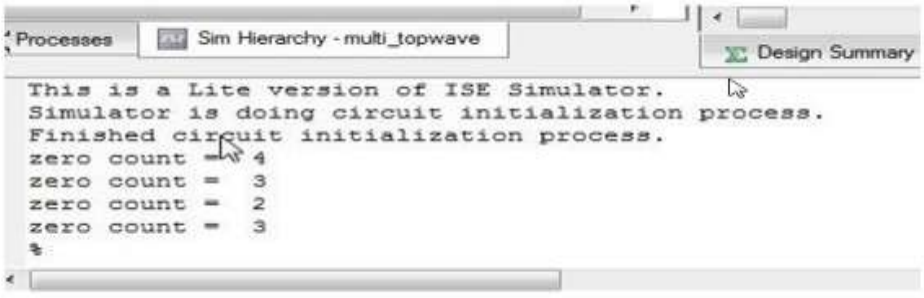

Fig. 10. No of zeroes for corresponding md bit

Performance Comparison of AM, CBPM, RBPM

Performance Analysis of Array Multiplier, Column and Row Bypass Multiplier shown in Table.1

PERFORMANCE	AM	CBPM	RBPM
TOTAL COMBO LOGIC	32	31	40
MAX FAN-OUT NODE	b[1]	b[0]	b[2]
MAX FAN-OUT	9	10	12
TOTAL FAN-OUT	115	118	145
AVG FANOUT	2.40	2.51	2.59
DELAY	13.909ns	15.806ns	15.37ns
TOTAL THERMAL POWER	69.11mw	69.01mw	68.93mw
CORE DYNAMIC TPD	0.05mw	0.03mw	0.03mw

Table 1. Performance Comparison Between AM, CBPM, RBPM

VI.CONCLUSION

In this paper, we propose an aging-aware reliable multiplier design with a novel adaptive hold logic (AHL) circuit. The multiplier is based on the variable-latency technique and can adjust the AHL circuit to achieve reliable operation under the influence of NBTI and PBTI effects. The multiplier is able to adjust the AHL to mitigate performance degradation due to increased delay. Note that in addition to the BTI effect that increases

transistor delay, interconnect also has its aging issue, which is called electro migration. If the aging effects caused by the BTI effect and electro migration are considered together, the delay and performance degradation will be more significant. Fortunately, our proposed variable latency multipliers can be used under the influence of both the BTI effect and electro migration. In addition, our proposed variable latency multipliers have less performance degradation because variable latency multipliers have less timing waste, but traditional multipliers need to consider the degradation caused by both the BTI effect and electro migration and use the worst case delay as the cycle period. The pipeline error recovery mechanism must guarantee that in the presence of Razor-detected errors, an incorrect value does not corrupt register or memory state.

VII.NOMENCLATURE

CBPM -COLUMN BYPASS MULTIPLIER

RBPM - ROW BYPASS MULTIPLIER

NBTI - NEGATIVE BIAS TEMPERATURE INSTABILITY

PBTI - POSITIVE BIAS TEMPERATURE INSTABILITY

AHL - ADAPTIVE HOLD LOGIC

VIII.REFERENCES

[1] H.-I.Yang,S.-C.Yang, W.Hwang,and C.-T.Chuang,“ Impacts of NBTI/PBTI on timing control circuits and degradation tolerant design in nano scale CMOS SRAM, ”*IEEE Trans.Circuit Syst.*,vol.58,no.6, pp.1239–1251,Jun.2011.

[2] R.Vattikonda, W.Wang, and Y.Cao,“ Modeling and minimization of pMOS NBTI effect for robust nanometer design,”in *Proc.ACM/IEEEDAC*,Jun.2004,pp.1047–1052.

[3] H.Abrishami, S.Hatami, B.Amelifard, and M.Pedram,“NBTI-aware flip-flop characterization and design,” in *Proc.44th ACMGLS VLSI*,2008,pp.29–34

[4] Y.Lee and T.Kim,“ A fine-grained technique of NBTI – aware voltage scaling and body biasing for standard cell based designs,” in *Proc. ASP- DAC*,2011,pp.603–608.

[5] N.V.Mujadiya,“Instruction scheduling on variable latency functional units of VLIW processors,” in *Proc. ACM/IEEE ISED*, Dec. 2011, pp.307–312.

[6] D.Mohapatra, G.Karakonstantis, and K.Roy, “Low-power process- variation tolerant arithmetic unit input-based elastic clocking,”in *Proc.ACM/IEEE ISLPED*,Aug.2007,pp.74–79.

[7] B.C.Paul, K.Kang, H.Kufluoglu, M.A.Alam, and K.Roy, “Impact of NBTI on the temporal performance degradation of digital circuits,” *IEEE Electron Device Lett.*,vol.26,no.8,pp.560–562,Aug.2005.

[8] R. Vattikonda, W. Wang, and Y. Cao, “Modeling and minimization of pMOS NBTI effect for robust nanometer design,” in *Proc. 43rd ,ACM/IEEEDAC*,Aug.2006,pp.1047–1052.

[9] D.Ernst *etal.*, “Razor: A low-power pipeline based on circuit-level timing speculation,”in *Proc.36th Annu. IEEE/ACMMICRO*, Dec. 2003, pp.7–18.

BIOGRAPHICAL NOTES

Ms.M.ARUNMOZHI DEVI is presently pursuing M.E final year in Electronics and Communication Engineering Department (specialization in VLSI design) from Theni Kammavar Sangam College of Technology, Theni, Tamilnadu, India.

Mr.S.SRINIDHI is working as an Assistant Professor in Electronics and Communication Engineering Department , from Theni Kammavar Sangam College of Technology, Theni, Tamilnadu, India.