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DESIGN OF FOLDING CIRCUIT AND SAMPLE AND HOLD FOR 6 BIT ADC

Prajeesh R[1], Manukrishna V R[2], Bellamkonda Saidilu[3]

[1]*Assistant Professor, ECE Department, SVNCE, Mavelikara, Kerala, (India)*

[2,3]*PhD Research Scholar, VIT University, Vellore, Tamil Nadu, (India)*

ABSTRACT

This paper describes the development of a 6 bit 100MHZ analog to digital converter with sample and hold based on a folding principle. The advantage of folding ADC compared to flash ADC is the reduced number of comparators. This ADC will have high speed and low power. Application of CMOS folding ADC can be found in high speed signal processing such as (oversampled) digitization of video signals. If we want to implement an 6 bit ash ADC we need 2^6 -1=63 comparators. But if we are implementing it in folding ADC we will divide the bits to MSB bits and LSB bits and is fed to a coarse ADC and fine ADC respectively. If we are dividing it into 2 bit coarse and 4 bit _ne, then the total number of comparators required is 2^2-1=3 for coarse and 15 for fine ADC also. That is total of 18 comparators which is much less when compared to flash ADC.

I. INTRODUCTION

An analog-to-digital converter (abbreviated ADC,A/D or A to D) is a device that uses sampling to convert a continues to a discrete time representation in digital form. The reverse operation is performed by a digital to analog converter (DAC). An ADC may also provide an isolated measurement such as an electronic device that converts an input analog voltage or current to a digital number proportional to the magnitude of the voltage or current.

An A/D converter converts a analog input (A) to a digital output(D).

$$D = f(A)$$

Figure 1.1 shows the input/ output characteristics where the analog input is approximated with the nearest smaller reference level. If digital output ism bit binary number then

$$D = 2mA=VREF$$

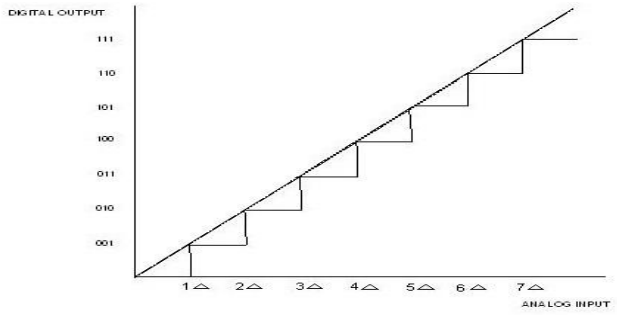

Figure 1.1: Input/Output Characteristics

Several characteristics define the dynamic performance of the ADC. The first is the resolution which is used to describe the minimum signal that the ADC can resolve. Resolution is limited by quantization noise and by the

harmonic distortion due to the finite number of bits in the ADC. The resolution is usually characterized by the signal-to-noise and distortion ratio (SNDR).Sampling rate or sampling frequency Fs is also an important characteristic of the ADC and defines the rate at which the analog input is sampled and converted to the digital domain. It is usually determined by the Nyquist bandwidth and must be larger than twice the input frequency. Another specification that is useful in characterizing the ADC is the effective resolution bandwidth (ERBW) which defines the frequency at which the ENOB drops by 0.5bit..

I. FOLDING ADC

High speed A/D converters have found many applications in communication circuits and network interfaces. The fastest architectures for A/D conversions are full ash ADC in which the whole A/D conversion finishes in single step. Applications of CMOS folding and interpolating A/D converters can be found in high-speed signal processing, such as (oversampled) digitalization of video signals. The advantage of CMOS technology over bipolar is that the A/D converter can be integrated on the same die as the digital signal processing part, resulting in a compact and cheap integrated system. The full ash ADC, however suffers from large die area when resolution is greater than 6bits. The number of comparators needed in full ash ADCs explodes exponentially with the resolution. The two or multiple-step ADCs require much less comparators than ash ADC but need two or several steps to finish conversion and they are therefore slow. Flash ADC converts the analog signal into digital by comparing it with a set of reference voltages. As the number of output bits increases, the circuit becomes bigger and the complexity of the layout increases. Hence, this architecture becomes impractical when higher resolution is required. Folding is a technique which reduces the number of comparators significantly by means of analog preprocessing circuit. This is proved to be efficient for high resolution ADC applications . By using folding techniques an A/D converter can be designed in which each comparator detects the zero crossings of the input signal through a number of quantization levels, thus reducing the number of comparators required for a given resolution. The number of comparators is reduced by the number of times that the input signal is folded by the folding stages.

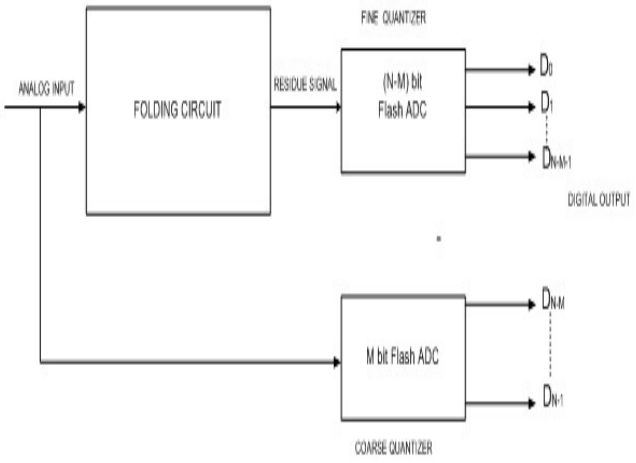

Figure 2: Folding ADCs

Figure 2 shows the block diagram of a two-step ADC consisting of a coarse quantizer, a digital to analog converter (DAC), a subtracter and a fine quantizer. The input signal is applied to a coarse quantizer ash ADC which generates the first M bits. Next, using an M-bit DAC, the output of the coarse quantizer is converted into an analog signal and subtracted from the input signal. The error signal is then quantized using a subsequent (N - M)-bit _ne quantizer ash ADC which generates the remaining bits. The die area of the ADC is reduced by performing the conversion in two (or more) clock cycles..

III. FOLDING PRINCIPLE

A simple way to make a high-speed A/D converter is to use a full-ash structure. This type of converter consists of an array of 2n - 1 comparators with n being the number of bits. Each comparator is connected with one input to the input voltage and with the other input to a reference voltage. This reference voltage is generally generated by a resistor ladder. The outputs of the comparators are fed into encoding logic that generate the data bits. The advantage of this full-ash converter is its ease of design and its high speed.The disadvantage of full-ash converters is that, if for example 8 b are needed, 255 comparators are required resulting in large chip area and power consumption. The folding technique need only a lower comparator count than a full-flash.

Figure 3 shows the block diagram of a folding A/D converter. The input voltage is applied to a analog preprocessing circuit depicted as the “folding circuit", and the output of this folding circuit is connected to a fine A/D converter. The input signal is also directly connected to a coarse A/D converter. For example, for a 8-bit converter requires only 31(fine) + 7(coarse)=38 comparators which is much less than the 255 required for ash ADC.

An N-bit folding ADC operates in a similar manner to a two-step ADC by quantizing the incoming signal through a coarse quantizer ash ADC and by generating a residue signal which is further quantized by a fine quantizer ash ADC . Coarse ADC converts the analog input to MSB bits and the LSB bits are generated using _ne ADC. The analog preprocessing circuit converts a full scale range and divides it into sub-ranges, the number of sub-ranges is defined as folding factor. Fine ADC converts this sub-range into LSB bits. The residue signal is generated by an analog folding block which reduces the dynamic range of the input signal by the folding factor F, thus resulting in number of comparators. The folding factor F is defined as the number of zero crossings in the folded signal for one full scale input signal. The coarse quantizer generates M bits while the fine quantizer generates the remaining (N-M) bits. The (N-M)bits fine ADC require 2N=F comparators. Folding architectures perform analog preprocessing to reduce the hardware while maintaining the one step nature of ash architectures. Folding ADCs have been shown to be an effective means of digitizing high-bandwidth signals at low-to-medium resolution with high sample rate. The analog folding architecture allows each comparator to detect more than one zero-crossing points; the number of zero crossings is referred to as the folding factor, and it reduces the number of comparators by nearly the same factor. In a folding ADC, the advantages of digital sampling of signals used in a full-ash system are combined with the component saving architecture of the two-step system.

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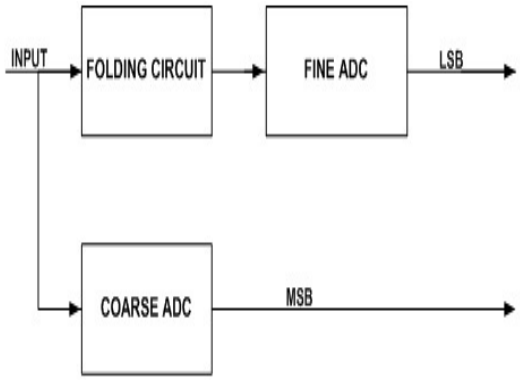

Figure 3: Block Diagram of Folding ADCs

The basic principle in folding is to generate a residue voltage through analog preprocessing and subsequently digitize that residue to obtain the least significant bits. The most significant bits can be resolved using a coarse flash stage at approximately the same time that the residue is sampled. The architecture uses an analog preprocessing block to transform the input signal into a repetitive set of output signals to be applied to the fine (ash) converter. The input signal is applied to a folding circuit. The folded signal at the output of this circuit is applied to a ash converter. Because the folded signal has a smaller range than the input signal, this ash converter can be small. For example, if the input signal is folded 8 times then the folded signal has only 1/8 of the range of the input signal. To get an 8-bit resolution with the folding A/D converter, the folded signal uses 5 bits or 31 comparators. These 5 bits will indicate the value of the conversion of the input signal into fine and coarse quantisation in the analog domain. input signal within the eight subranges of the input signal. A separate coarse quantisation is required to _nd out in which subrange the input signal is located. Because there are eight subranges the coarse quantisation requires 3-bit or 7 comparators. The number of comparators of the folding A/D converter brings it back from 255 to 38 comparators. The folding structure is different from the two-step principle in that it performs the conversion of the input signal into fine and coarse quantisation in the analog domain.

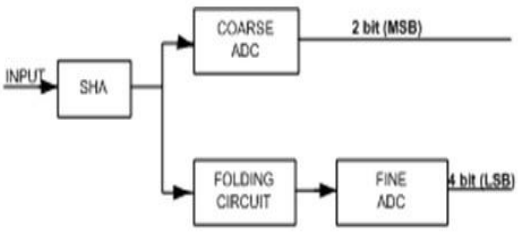

Fig 4. Folding ADC

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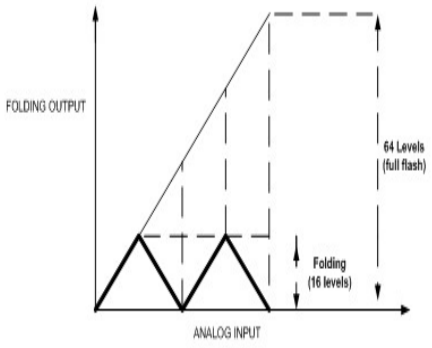

Fig 5 . Transfer Curve for Folding ADC

IV. 6 BIT FOLDING ADC

Folding circuit is employed to reduce the number of comparators which is accomplished by corrugating the input signal along the reference voltages. Figure 5 shows the transfer curve for a folding circuit with folding factor

4. As the input increases linearly from zero to 1.2V, the differential output initially increases subsequently crosses zero voltage at Vref1, then folds back and crosses zero when input signal is Vref2. This repeats and eventually a fourfold signal with four zero crossings is generated. The comparator outputs

represent the input signal in a cyclic binary Gray code or a thermometer-like code that is eventually converted to a compact digital representation of the analog input. The conversion requires a logic block that can be realized as a read-only memory (ROM).

Device mismatch creates INL and DNL errors in standard design architecture for ash and folding A/D converters and it is a fundamental drawback in making high-resolution converters. Wider resistors in the reference ladder and larger transistors in the input preamplifiers will improve the precision, but at the cost of increased die size, power dissipation and decreased sample rate. The main disadvantage of the folding ADC is the reduced bandwidth due to the internal multiplication of the input signal frequency with the

folding rate. This problem can be solved employing either a front-end T/H circuit or a distributed T/H circuit after the first folding stage. In 6-bit folding ADC , a total of 18 comparators (3 for coarse and 15 for fine quantizer)are needed while a 6-bit full flash ADC needs 63 comparators. Generally ,a folding ADC reuses comparators so that the total number of comparators can be reduced by a folding factor ie.,4 in this example. In this design we are not using multiple folders. Figure 3 shows the transfer curve of the folding circuit with a folding factor of four

Folding circuit is employed to reduce the number of comparators which is accomplished by corrugating the input signal along the reference voltages.Figure 3 shows the transfer curve for a folding circuit with folding factor 4. As the input increases linearly from zero to 1.2V, the differential output

initially increases subsequently crosses zero voltage at Vref1, then folds back and crosses zero when input signal is Vref2. This repeats and eventually a fourfold signal with four zero crossings is generated. The comparator outputs represent the input signal in a cyclic binary Gray code or a thermometer-like code that is eventually converted to a compact digital representation of the analog input. The conversion requires a logic block that can be realized as a read-only memory (ROM).

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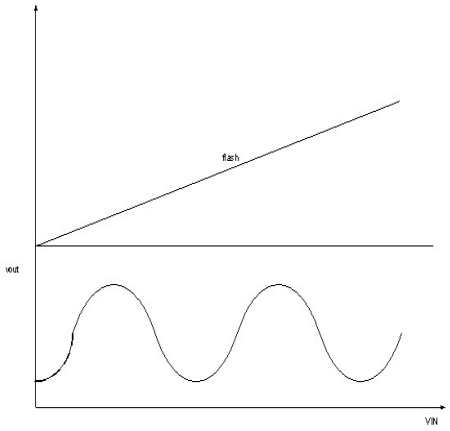

Fig 6. Transfer Curve for Factor 4

Device mismatch creates INL and DNL errors in standard design architecture for ash and folding A/D converters and it is a fundamental drawback in making high-resolution converters. Wider resistors in the reference ladder and larger transistors in the input preamplifiers will improve the precision, but at the cost of increased die size, power dissipation and decreased sample rate. The main disadvantage of the folding ADC is the reduced bandwidth due to the internal multiplication of the input signal frequency with the
folding rate. This problem can be solved employing either a front-end T/H circuit or a distributed T/H circuit after the first folding stage.

V. DESIGN OF FOLDING CIRCUIT AND COMPARATOR

Figure 7 shows the scheme for the CMOS folding circuit(a 4 times folder) for the use in a 6-bit folding circuit. The folding circuit consists of four differential amplifiers and an extra current source. The reference voltages Vr1,Vr2,Vr3,Vr4 are generated using a reference ladder network shown in Figure 8. We may use an extra differential amplifier instead of the current source. Here the four differential pairs process the difference between Vin and Vr1,...,Vr4 and their output currents are summed at nodes X and Y. The outputs of the adjacent stages are added with opposite polarity(e.g., as Vinincreases,Q1 pulls node X low while Q2 pulls node Y low). Current source I5shifts VY down by IR. Figure 9 shows the extra differential amplifier usedinstead of the current source.

The operation of the folding circuit is explained by considering the in-put/output characteristic, plotted in Figure 310 For Vin well below Vr1 ,

Q1-Q4 are OFF,Q5-Q8 are ON , I2 and I4 ow through RC1, I1 , I3 and I5flow through RC2. As Vin increases, Q1 begins to turn ON, while Q2-Q4 remains OFF(if Vr1,...,Vr4 are sufficiently far from each other). For Vin=Vr1, Q1 and Q5 share current I1 equally yielding VX=VY. As Vin exceeds Vr1 by several VT ,Q5 turns OFF , allowing VX and VY to reach Vmin and Vmax respectively. As Vin approaches Vr2, Q2 begins to turn ON and circuit behaves in a similar manner as before. Considering the differential output,(VX-VY),the resulting characteristics exhibits folding points at (Vr1+Vr2)/2 , (Vr2+Vr3)/2 , etc. As Vin goes from below Vr1 to above Vr4, the slope of(VX-VY) changes sign four times, hence we say circuit has a folding factor of four.

In the folding characteristic shown in Figure11 ,if the input goes from zero to full scale once, the output goes from Vmin to Vmax four times; i.e., a folding factor of n results in a frequency multiplication by n. Thus the band- width required of the folding circuit is n times that of the maximum input

frequency. As a result in high-speed systems the folding factor is typically between 2 and 4. Another important property of folding characteristic is its substantial nonlinearity. The non-linearity errors in folding characteristic also depend on the frequency of operation. At high speeds, the rate of change

of signals become comparable with the intrinsic time constants of the circuit thus causing the “rounding"of the characteristic at the folding points and hence increasing the nonlinearity. One solution to avoid this nonlinearity is to use multiple folders.

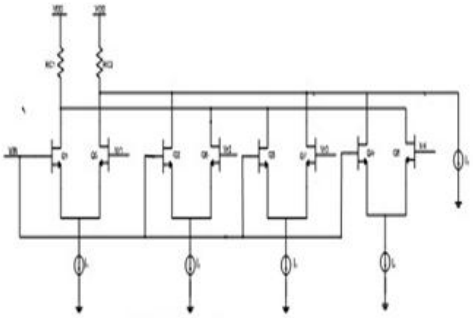

Fig 7. Folding Circuit

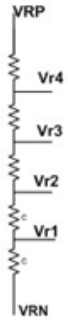

Fig 8. Reference Voltage Generation

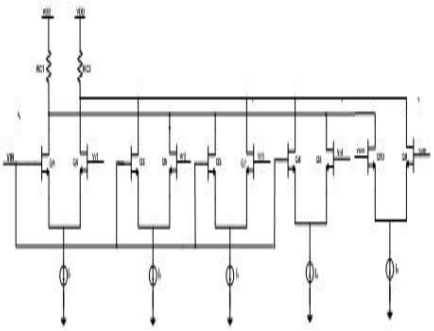

Fig 9. Folding Circuit

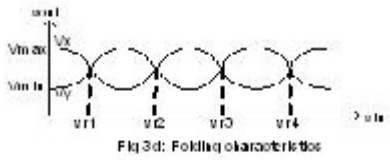

Fig 10 . Folding Chara

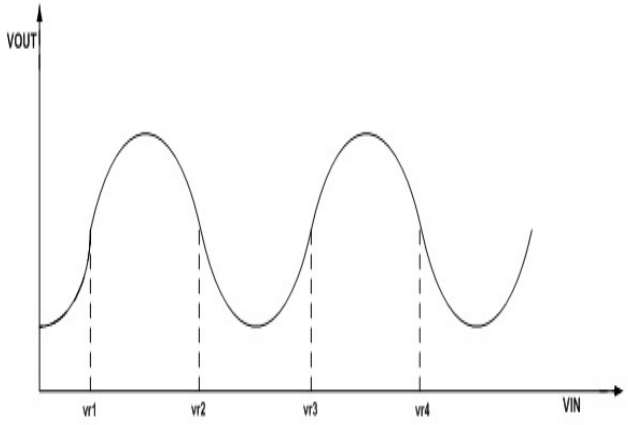

Fig 11. Transfer Charachteristics of Folding Circuit for a Folding Factor 4

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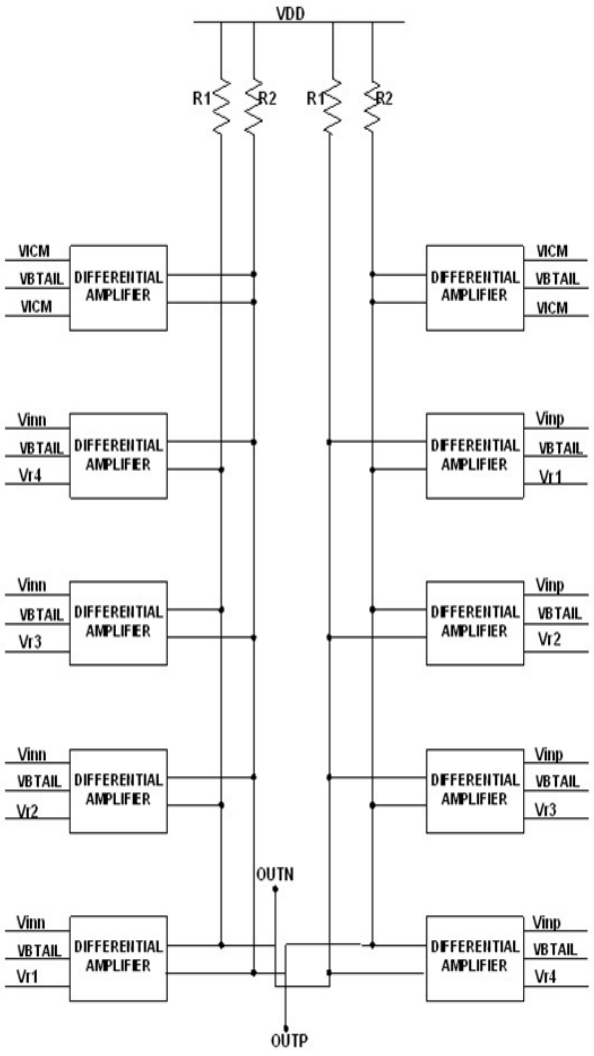

Fig 12 Differential Implementation of Folding Circuit

VI. DESIGN OF SAMPLE AND HOLD

If we are directly feeding an analog signal to an ADC, the ADC cannot make correct decision because the analog input is changing the value instantaneously, so we are sampling the value of an analog input and holding the value for sometime so that adc get enough time to take decision. For this we are making use of sample and hold circuitry. Here we are providing two common modes input common mode and output common mode. During the sample mode the switches s1l and sle gets closed and switch s2 is opened and the capacitors c1 and c2 gets charged to Vin-Vincm. During the hold mode the switches s1l and s1e gets opened and switch s2 gets closed. During this time the output gets charged to Voutcm-(Vin-Vincm).

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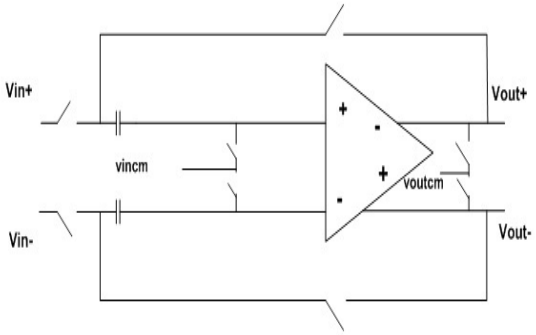

Fig 13 . Sample and Hold Circuit

VII. IMPLEMENTATION IN CADENSE

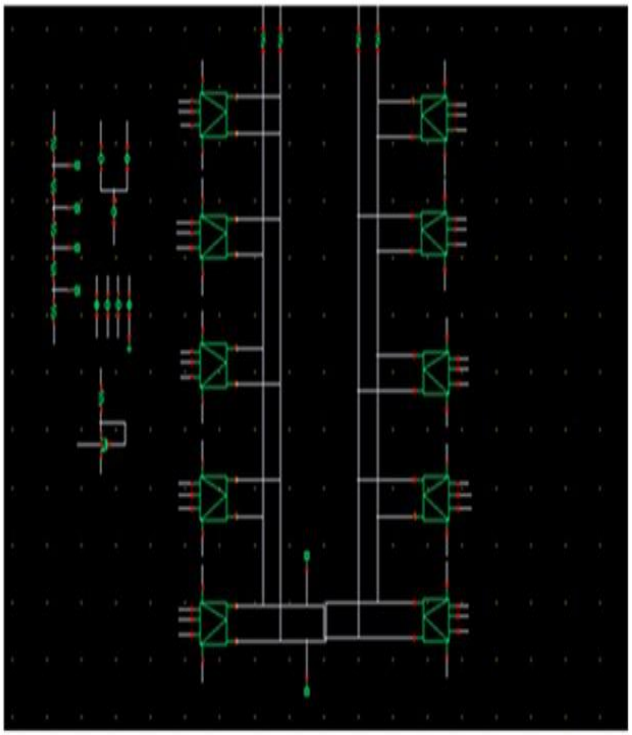

Fig 13 Implementation of Folding Circuit in Cadence

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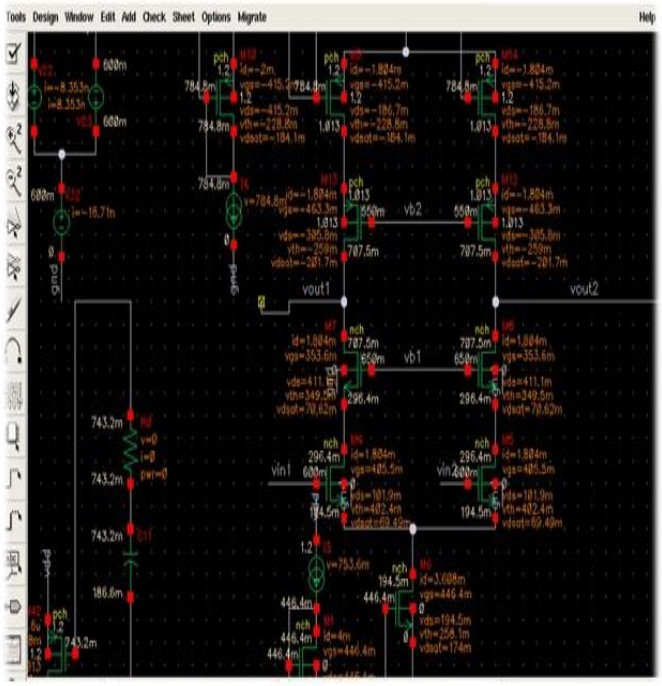

Fig 15.Sample and Hold Circuit in Cadence

VIII. SIMULATION RESULTS

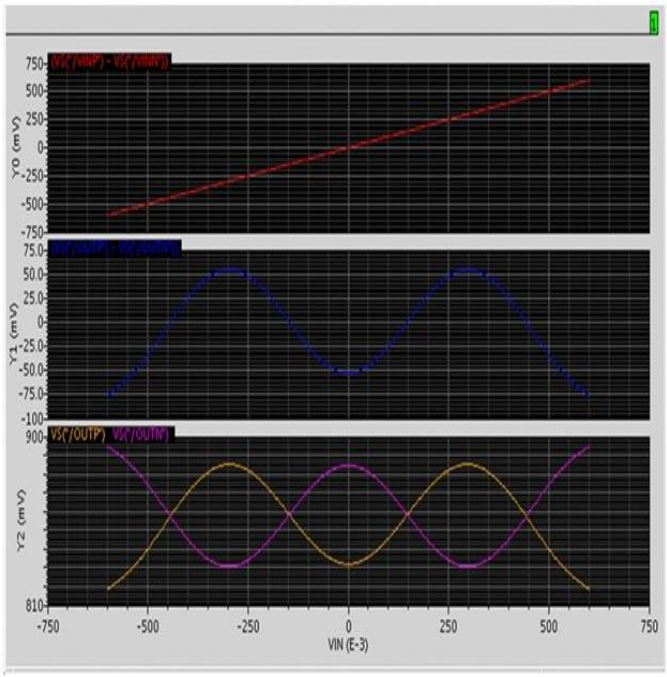

Fig 14. Simulation Result for Folding Circuit

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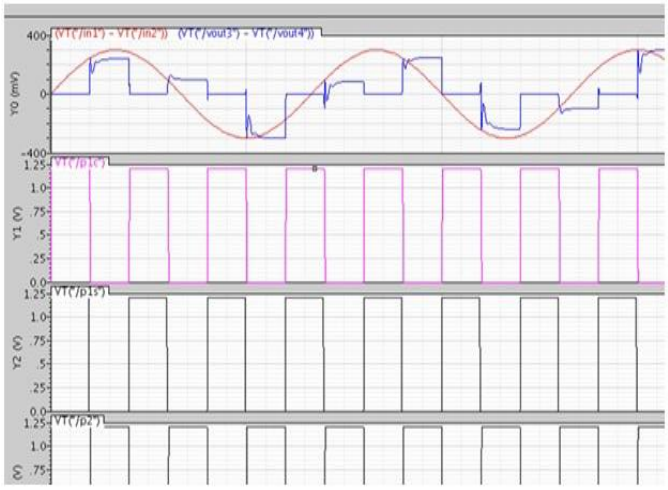

Fig 15 Simulation Result of Sample and Hold

IX. CONCLUSION

The folding circuit is designed for a folding factor of four. The folding ADC is designed for 6bit resolution {4bit for _ne and 2bit for coarse. The low power dissipation of the ADC is the main advantage of this technology in comparison with other state-of-art technologies (Bipolar or even CMOS). The analog circuitry is simplified at the expense of digital complexity. By doing so, the overall performance improves with processing speed and digital density, thus, aligning precisely with the benefits of CMOS scaling. Therefore, as technology shrinks, these circuits will scale accordingly, port easily, and will not

super performance degradation.

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