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DTMF BASED ELECTRONIC VOTING MACHINE

Alok Kumar Tiwari[1], Shivam Raghav[2], Tanzeem-Ul-Haq[3] ,Pallavi Gupta[4]

[1, 2,3] *Students, Electrical Engineering Department Greater Noida Institutes of Technology, Gr.Noida, (India)*

[4] *Assistant Professor, Electrical Engineering Department Greater Noida Institutes of Technology, Gr. Noida, (India)*

ABSTRACT

In this research, an electronic votingscheme using Cell Phone technology is presented. This idea is the complete solution for conducting secure election and it help to stop 100% booth capturing. India is world's largest democracy. Fundamental right to vote or simply voting in elections forms the basis of Indian democracy. In India all earlier elections a voter used to cast his vote by using ballot paper. This is a long, time-consuming process and very much prone to errors.

This situation continued till election scene was completely changed by electronic voting machine. No more ballot paper, ballot boxes, stamping, etc. all this condensed into a simple box called ballot unit of the electronic voting machine. Cell phone based voting machine is capable of saving considerable printing stationery and transport of large volumes of electoral material. It is easy to transport, store, and maintain. It completely rules out the chance of invalid votes. Its use results in reduction of polling time, resulting in fewer problems in electoral preparations, law and order, candidates' expenditure, etc. and easy and accurate counting without any mischief at the counting centre.

***Keywords**: DTMF, EVM(Electronic Voting Machine), Memory Storage Device EEPROM, Microcontroller, Cell Phone.*

I. INTRODUCTION

Today, only about 1 percent of the population votes at polling places on hand counted paper ballots, but this figure is misleading. There are many elections conducted on optical mark-sense ballots that are actually hand counted, and many jurisdictions that use lever voting machines process absentee ballots by hand. The aim of our project is to design & develop a mobile based voting machine. In this project user can dial the specific number from any land line or mobile phone to cast his vote. Once the user is connected to the voting machine he can enter his password & choice of vote. If he has entered a valid choice & password his vote will be caste with two short duration beeps. For invalid password/choice long beep will be generated. User is allotted 15 seconds to enter his password & choice. A reset button is provided for resetting the system. A total key is provided to display the result. We have also used non-volatile memory for storing all data. EEPROM will preserve all information in case of power failure. In this project all information is transmitted through DTMF tones. The major block & their functions are described in details below.

II. DTMF DECODER

In DTMF decoder circuit we use IC 8870. IC 8870 converts the dual tones to corresponding binary outputs.

III. DTMF SIGNALLING

AC register signalling is used in DTMF telephones, here tones rather than make/break pulse are used for dialling, eachdialled digit is uniquely represented by a pair of sine waves tones. These tones (one from low group for row and another from high group for column) are sent to the exchange when a digit is dialled by pushing the key, these tone lies within the speech band of 300 to 3400 HZ, and are chosen so as to minimize the possibility of any valid frequency pair existing in normal speech simultaneously. Actually, this minimisation is made possible by forming pairs with one tone from the higher group and the other from the lower of frequencies. A valid DTMF signal is the sum of two tones, one from a lower group (697-940 Hz) and the other from a higher group (1209-1663 Hz). Each group contains four individual tones.This scheme allows 10 unique combinations. Ten of these code represent digits 1 through 9 and 0tones in DTMF dialling are so chose that none of the tones is harmonic of are other tone. Therefore is no change of distortion caused by harmonics. Each tone is sent as along as the key remains pressed. The DTMF signal contains only one component from each of the high and low group. This significantly simplifies decoding because the composite DTMF signal may be separated with band pass filters into single frequency components, each of which may be handled individually.

IV. MICRO-CONTROLLER AT89S51

The AT89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K bytes of in-system programmable Flash memory. The device is manufactured using Atmel's high-density non-volatile memory technology and is compatible with the industry- standard 80C51 instruction set and pin out. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional non-volatile memory programmer. By combining a versatile 8-bit CPU with in-system programmable Flash on a monolithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

The AT89S51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines,Watchdog timer, two data pointers, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset.

V. PIN DIAGRAM

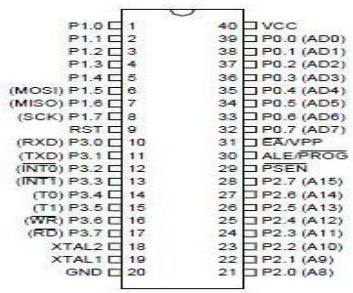

Fig No.Pin Diagram of AT89S51

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VI. PIN DESCRIPTION

- **VCC:** Supply voltage.
- **GND:** Ground.
- **Port 0:** Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs. Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups. Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification.

VII. EXTERNAL PULL-UPS ARE REQUIRED DURING PROGRAM VERIFICATION

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

Table 1.1 : Port 1 Configuration

- **Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL) because of the internal pull-ups.
- **Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL) because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Table 1.2: Port 3 Configuration

- **RST:** Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.
- **ALE/PROG:** Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during

each access to external data memory. If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH.

- **PSEN:** Program Store Enable (PSEN) is the read strobe to external program memory. When the AT89S51 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.
- **EA/VPP:** External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset. This pin also receives the 12-volt programming enable voltage (VPP) during Flash programming.
- **XTAL1:** Input to the inverting oscillator amplifier and input to the internal clock operating circuit.
- **XTAL2:** Output from the inverting oscillator amplifier.

VIII. DTMF RECEIVER IC CM8870

Processor brain decodes instructions and generate control signal for various sub units. It has full control over the clock distribution unit of processor.The CAMD CM8870/70C provides full DTMF receiver capability by integrating both the band-split filter and digital decoder functions into a single 18-pin DIP, SOIC, or 20-pin PLCC package. The CM8870/70C is manufactured using state-of-the-art CMOS process technology for low power consumption (35mW, MAX) and precise data handling. The filter section uses a switched capacitortechnique for both high and low group filters and dial tone rejection. The CM8870/70C decoder uses digital counting techniques for the detection and decoding of all 16 DTMF tone pairs into a 4-bit code. This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

8.1 Pin Diagram

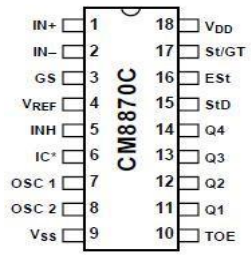


Fig No. Pin Diagram of CM8870C

IX. ATMEL 24C16

The AT24C01A/02/04/08/16 provides 1024/2048/4096/8192/16384 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 128/256/512/1024/2048 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT24C01A/02/04/08/16 is available in space-saving 8-pin PDIP, 8-lead JEDEC SOIC, 8-lead MAP and 8-lead TSSOP packages and is accessed via a 2-wire serial interface.

9.1 Pin Diagram

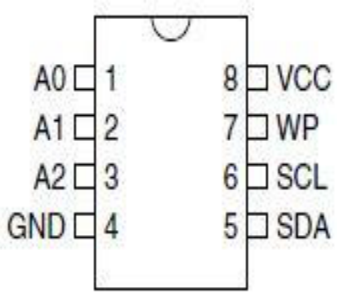


Fig No. Pin Diagram of AT 24C16

X. VOLTAGE REGULATOR

Voltage regulator ICs are available with fixed (typically 5, 12 and 15V) or variable output voltages. The maximum current they can pass also rates them. Negative voltage regulators are available, mainly for use in dual supplies. Most regulators include some automatic protection from excessive current and overheating (thermal protection). Many of fixed voltage regulator ICs has 3 leads. They include a hole for attaching a heat sink if necessary.

10.1 Diagram

Fig No. 7805 Voltage Regulator

XI. LCD DISPLAY

This is the first interfacing example for the Parallel Port. We will start with something simple. This example doesn't use the Bi-directional feature found on newer ports, thus it should work with most, if not all Parallel Ports. These LCD Modules are very common these days, and are quite simple to work with, as all the logic required to run them is on board.

The LCD panel's Enable and Register Select is connected to the Control Port. The Control Port is an open collector / open drain output. While most Parallel Ports have internal pull-up resistors, there is a few which don't. Therefore by incorporating the two 10K external pull up resistors, the circuit is more portable for a wider range of computers, some of which may have no internal pull up resistors.

We make no effort to place the Data bus into reverse direction. Therefore we hard wire the R/W line of the LCD panel, into write mode. This will cause no bus conflicts on the data lines. As a result we cannot read back the LCD's internal Busy Flag which tells us if the LCD has accepted and finished processing the last instruction. This problem is overcome by inserting known delays into our program. The 10k Potentiometer controls the contrast of the LCD panel. Nothing fancy here. As with all the examples, I've left the power supply out. You can

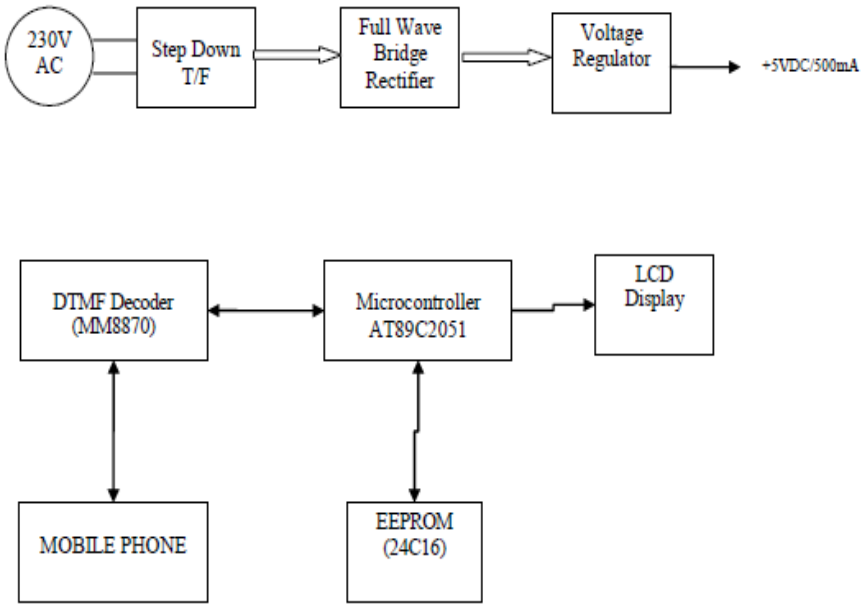
use a bench power supply set to 5v or use an onboard +5 regulator. Remember a few de-coupling capacitors, especially if you have trouble with the circuit working properly.

XII. WORKING OF PROJECT

The working of this project is controlled by a microcontroller ATMEL AT89C51 and a DTMF decoder CM8870 is used for decoding key tones of cell phone and EEPROM is used for memory storage. The project works in the following ways:

1. Switch on power supply.
2. Message wait will appear on LCD.
3. Type #22 followed with candidate number to enter the vote where 22 is the password.
4. If vote is casted then "vote casted successfully" on the LCD & if not then "invalid vote try again" will appear.
5. To check the number of vote press the button on the PCB and number of votes of each candidate & total number of vote will appear on LCD.
6. A reset key is present to reset the microcontroller.

XIII. BLOCK DIAGRAM



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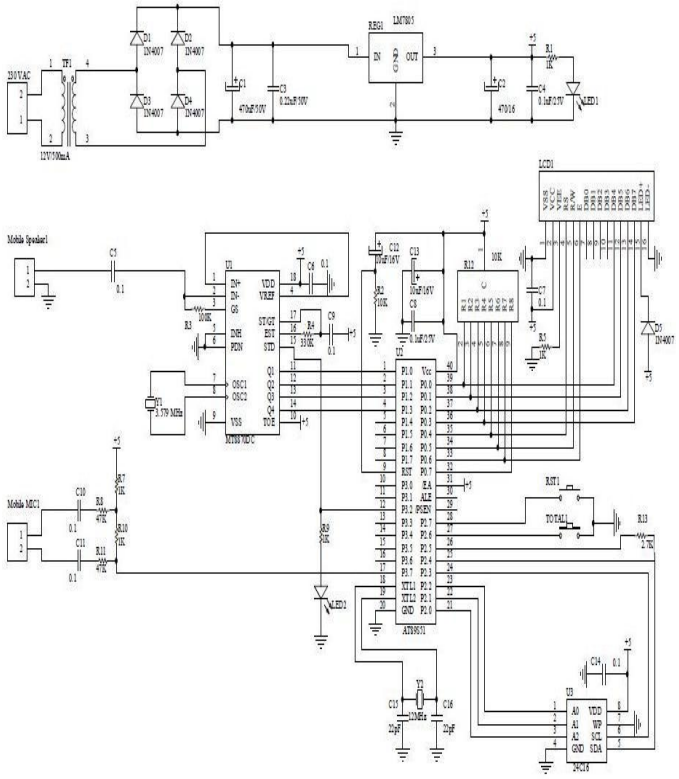
XIV. CIRCUIT DIAGRAM



XV. CONCULSION

15.1 Future Scope

1. Number of candidates could be increased by using other microcontroller.
2. It could be interfaced with printer to get the hard copy of the result almost instantly from the machine itself.
3. It could also be interfaced with the personal computer and result could be stored in the central server and its backup could be taken on the other backend servers.
4. Again, once the result is on the server it could be relayed on the network to various offices of the election conducting authority. Thus our project could make the result available any corner of the world in a matter of seconds

XVI. AREA OF APPLICATIONS

1. Fast track voting which could be used in small scale elections, like resident welfare association, “panchayat” level election and other society level elections.
2. It could also be used to conduct opinion polls during annual share holdersmeeting.
3. It could also be used to conduct general assembly elections where number of candidates are less than or equal to eight in the current situation.
4. It is used in various TV serials as for public opinion.

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