

# OTRA BASED R-2R LADDER AND WEIGHTED RESISTOR DAC REALIZATIONS

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## ABSTRACT

*This paper presents realization of R-2R ladder and weighted resistor digital to analog converters (DACs) using the Operational Trans Resistance Amplifiers (OTRA). These circuits use a single OTRA and are therefore power efficient. The functionality of the proposed converters is verified through SPICE simulations using CMOS based implementation of the OTRA. The circuits are shown to be 3-bit accurate using DNL and INL analysis. Other parameters like offset have also been computed. Through DNL and INL analysis, monotonicity of both configurations has been preserved.*

**Keywords:** CMOS based OTRA, Digital-to-Analog Conversion, OTRA, Resistive Ladders, Weighted Resistors

## I. INTRODUCTION

Digital to Analog converters (DACs) are used in wide range of applications. It is employed - in audio amplifier to produce DC voltage gain with microcontroller commands; to provide dynamic calibration for gain and voltage offset for accuracy in test and measurement system; to change voltage dynamically during operation of the system circuits that convert digital input to analog signals and in digital potentiometers. The DACs are typically realized with operational amplifier which has constant gain-bandwidth product and lower slew rate therefore their high frequency operations are limited. The current mode active blocks on the other hand possess gain independent of gain and better slew rate. The research therefore has gained momentum towards developing applications based on current mode active blocks.

The OTRA inherits all the advantages offered by current mode techniques, and has emerged as an alternate analog building block for developing various applications [1-8]. The OTRA is a high gain current input voltage output device. Due to low impedance input and output terminals, limitations on the response by the time constants of the capacitors are reduced. The device is unaffected by stray capacitances due to virtually grounded inputs [3]. Ideally, the Transresistance gain of OTRA approaches infinity and external negative feedback must be used which forces the input currents to be equal. The OTRA has not been used for realization of DAC to the best of authors' exposure in the field.

This paper aims at putting forward OTRA based DAC realizations. The paper is arranged in five sections. The terminal properties and its CMOS schematic is briefly discussed first in section 2 and is followed by proposed

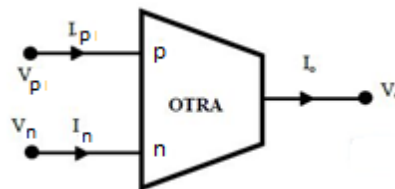
DAC configurations. Simulation results for functional verification and performance are given in section 3 and conclusions are drawn in section 4.

**II. CIRCUIT DESCRIPTION**

The OTRA is a three terminal current mode analog device with two low-impedance input terminals and one low-impedance output terminal. The input terminals of the OTRA are virtually grounded. The input and output terminal of an OTRA can be characterized by the matrix of (1)

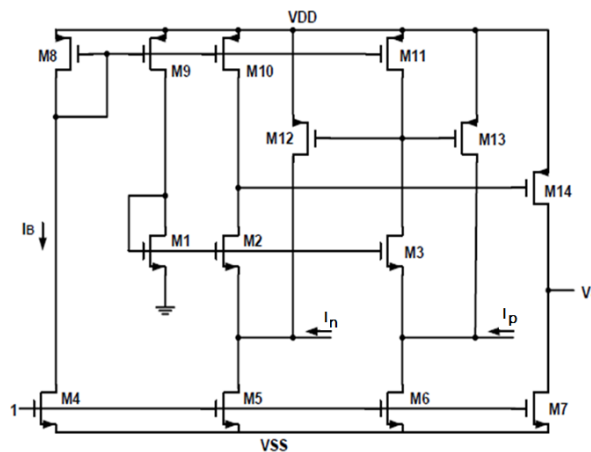
$$\begin{bmatrix} V_p \\ V_n \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_o \end{bmatrix} \tag{1}$$

Where  $R_m$  is the Transresistance gain of the ideal OTRA. Ideally the value of the  $R_m$  gain is very high; therefore the OTRA has to be used in negative feedback configuration for linear applications



**Fig.1 the OTRA block**

The CMOS based schematic of OTRA [6] is shown in Fig. 2. The transistors M1 – M13 form current differencing circuit and provide a virtual ground at p and n terminals whereas common source amplifier (M14) provides high gain.



**Fig.2 OTRA Block using CMOS implementation [6]**

The proposed OTRA based R-2R and weighted resistor 3 – bit DAC realizations are shown in Fig. 3. Both the circuits use single OTRA and three switches. The number of resistors in proposed R-2R DAC and weighted resistor DAC are eight and four respectively. The output voltage  $V_o$  for Fig. 3a is computed as:

$$V_o = i_{total} \cdot R_f \tag{2}$$

Where  $i_{total}$  is, the sum of currents entering at p terminal of OTRA, selected by the digital input given by

$$i_{total} = \sum_{k=0}^{N-1} D_k \cdot \frac{V_{in}}{2^{N-k}} \cdot \frac{1}{2R} \tag{3}$$

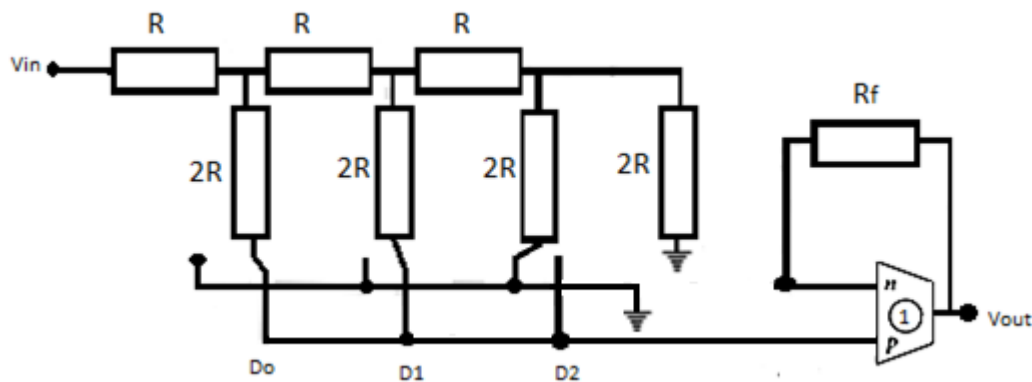
Where  $D_k$  is the  $k^{th}$  bit of the input word that is either 0 or 1.

The output voltage  $V_o$  for Fig. 3b can be computed as:

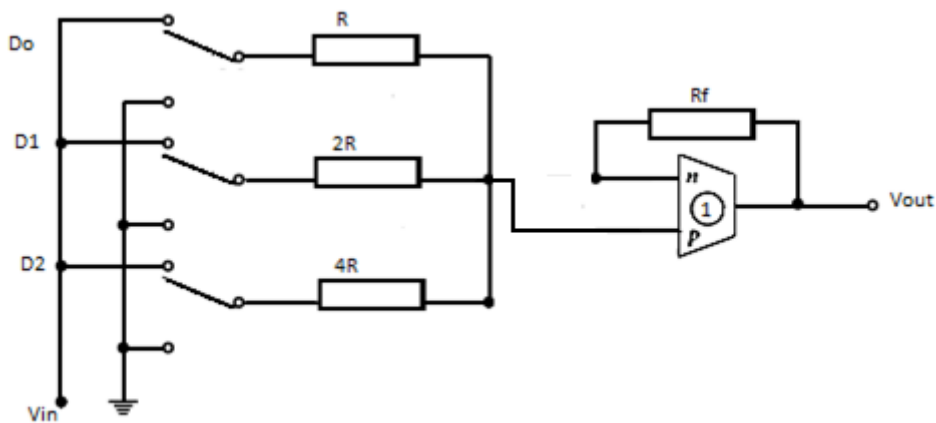
$$V_o = i_{total} \cdot R_f \tag{4}$$

Where,

$$i_{total} = \sum_{k=0}^{N-1} D_k \cdot \frac{V_{in}}{2^{N-k-1}} \cdot \frac{1}{R} \tag{5}$$



(a)



(b)

**Fig.3 Proposed OTRA based (a) R-2R and (b) weighted resistor DAC realizations.**

Further, we delineate the differences between the weighted DAC and the R-2R realizations. It can be seen that while both circuits make use of one active block each, the weighted DAC comprises of fewer passive components. Both converters being monotonic, the weighted DAC has a higher error in output value than its R-2R counterpart circuit. While the weighted DAC is an optimum choice of converter for low bit circuits, for high

number of bits it has the problem of a wide range of resistor values  $R$  to  $2^{N-1}R$  with required precision and also which tracks over a wide temperature range. The R-2R in general, takes care of this problem by only employing resistors of two values-  $R$  and  $2R$ .

### III. SIMULATION RESULTS

The operation and performance of proposed DAC realizations of Fig 3 are verified through SPICE simulation using  $0.5 \mu\text{m}$  CMOS technology parameters and power supply of  $\pm 1.5\text{V}$ . The proposed circuit is shown as 3-bit accurate after careful analysis of DNL and INL parameters. Offset for both the R-2R and weighted resistor circuits have also been calculated to be near negligible. The component values for the R-2R circuit are  $R = 1\text{k}\Omega$ ,  $R_f = 2\text{k}\Omega$ ,  $V_{in} = 5\text{V}$  and the component values for the weighted resistor DAC are  $R = 1\text{k}\Omega$ ,  $R_f = 2.5\text{k}\Omega$ ,  $V_{in} = 5\text{V}$ . The theoretical, simulated output voltage and relative error for both proposed DACs have been recorded in Tables 1 and 2. Output voltages have also been plotted in Figs. 4 (a) and (b). As can be seen from Tables 1 and 2 that the error percentage is less than 0.1 % for the R-2R DAC and less than 1% for the weighted DAC.

**Table 1: Output voltage for proposed R-2R DAC circuit**

Digital Input	$V_{OUT}$ (Theoretical)	$V_{OUT}$ (Simulated)	%Error
000	0	$10^{-30}$	Negligible
001	0.625	0.624701	0.04
010	1.25	1.2494	0.04
011	1.875	1.8739	0.05
100	2.5	2.4988	0.04
101	3.125	3.1230	0.06
110	3.75	3.7477	0.06
111	4.375	4.3720	0.06

**Table 1: Output voltage for proposed weighted resistor DAC circuit**

Digital Input	$V_{OUT}$ (Theoretical)	$V_{OUT}$ (Simulated)	%Error
000	0	$10^{-30}$	Negligible
001	3.125	3.1212	0.12
010	6.25	6.2425	0.12
011	9.375	9.3635	0.12
100	12.5	12.485	0.12
101	15.625	15.606	0.12
110	18.75	18.7275	0.12
111	21.875	21.8485	0.12

DNL analysis has also been done and has been shown in fig 5. Both the R-2R and weighted resistor configurations have a DNL of the order of  $10^{-3}$  and  $10^{-4}$  respectively. INL analysis has also been done and has been shown in fig 6. Both the R-2R and weighted resistor configurations have an INL of the order of  $10^{-3}$ .

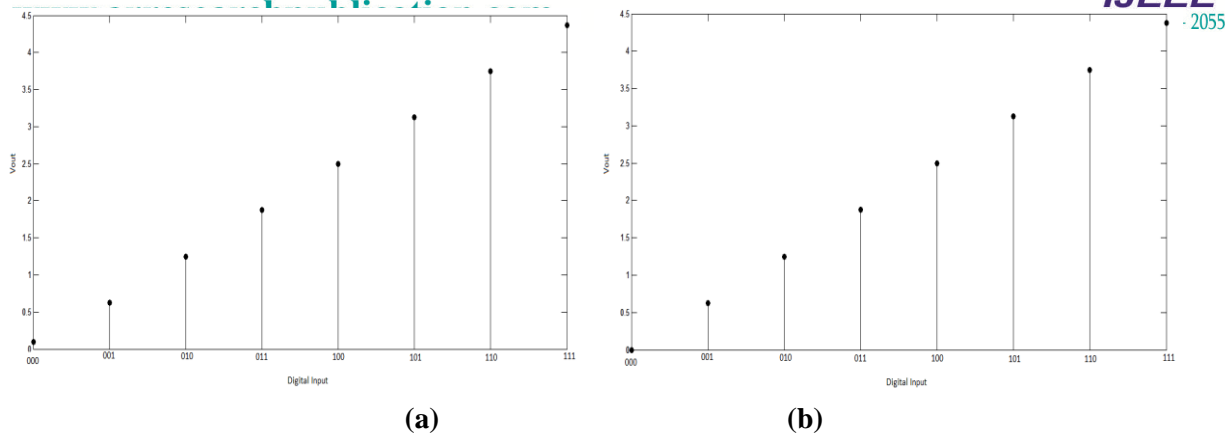


Fig. 4 Output voltages for proposed (a) R-2R and (b) weighted resistor DAC

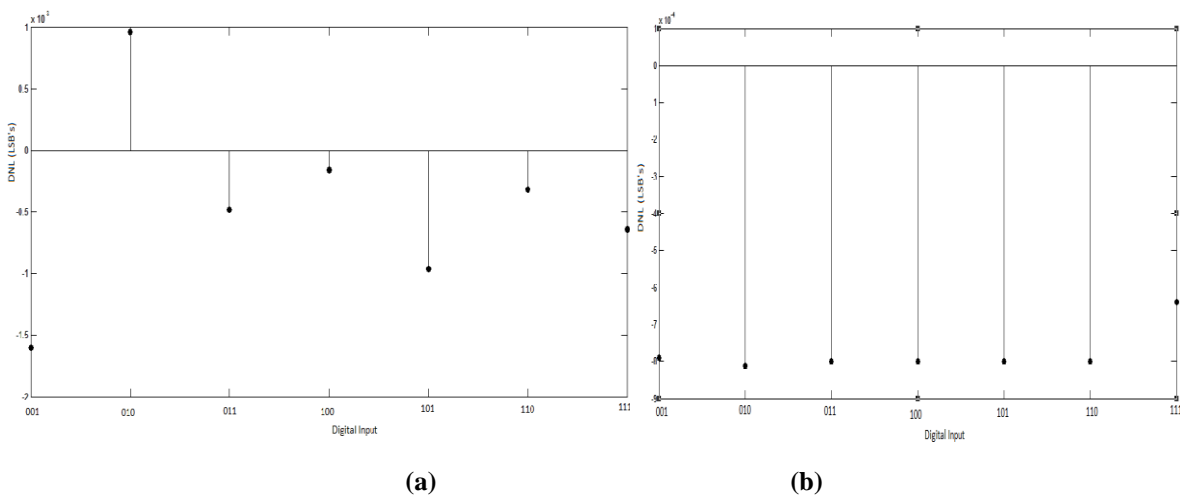


Fig. 5 DNL for proposed (a) R-2R and (b) weighted resistor DAC

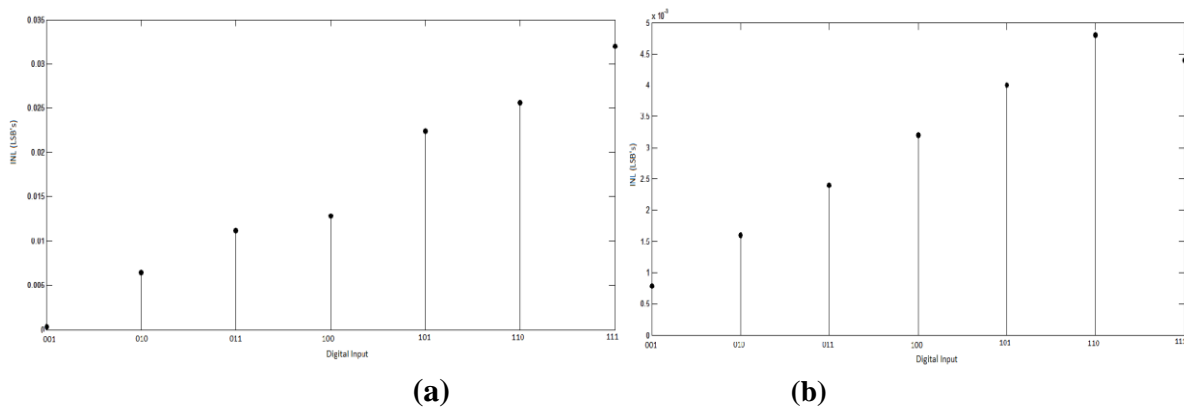


Fig. 6 INL for proposed (a) R-2R and (b) weighted resistor DAC

#### IV. CONCLUSION

New realizations of OTRA based R-2R and weighted DAC's have been presented. Both configurations are shown to be 3-bit accurate. They are monotonic through DNL and INL analysis. They provide advantages over existing circuits in the form of improved DNL and INL measurements. By using the OTRA, gain-bandwidth independence is achieved. We are also able to achieve optimum slew rate and negligible parasitic effects.

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