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INVESTIGATION & ANALYSIS OF LINE-INTERACTIVE SINGLE-PHASE DYNAMIC VOLTAGE RESTORER WITH SAG DETECTION ALGORITHM

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ABSTRACT

The development of a line-interactive single-phase dynamic voltage restorer (DVR) with a novel sag detection algorithm is described in this paper. The developed detection algorithm has a hybrid structure composed of an instantaneous detection part and the root-mean-square (rms) variation detection part. The source voltage passes through the instantaneous sag detection part. If in-stantaneous sag is detected, the rms variation detector-1 is selected to calculate the rms variation. The rms variation detector-2 is selected when the instantaneous sag occurs under the operation of the rms variation detector-1. The feasibility of proposed algorithm was verified through computer simulations and experimental works with a 3-kVA-rating prototype of line-interactive DVR. The line-interactive DVR with the proposed algorithm can compensate the input voltage sag or interruption within 2.0 ms delay. The developed DVR can be effectively utilized for the sensitive loads, such as a computer, communication device, and automation device.

Index Terms: Discrete Fourier transform (DFT), dynamic voltage restorer (DVR), line-interactive, phase-locked loop (PLL), root mean square (rms) variation detector, voltage sag or interruption.

I. INTRODUCTION

Recently, computer, communication devices, and automation devices have come into wide use in the office, industry, and even home. These devices, which operate continuously during 24 h, require highly reliable input power. Supplying unreliable input power to these devices brings severe loss to the customer. One of the input power disturbances is the voltage sag or interruption due to the fault in the interconnected power system [1], [2]. The compensator for the voltage sag or interruption is called the dynamic voltage restorer (DVR) [3]. DVR for the voltage sag does not require energy storage unit, while DVR for voltage interruption requires it. DVR is divided into two types with reference to the connection pattern. DVR connected in series with load through the transformer is the most common structure [4]. One severe disadvantage of this configuration is high system loss due to the continuous operation. Another disadvantage is the delicate protection due to the series connection of the system. DVR, which is connected in parallel with load and operated with the line-interactive scheme, is another structure. One remarkable advantage is a relatively low system rating and loss because the DVR operates only for disturbance time. However, a disadvantage is the compensation delay between the disturbed point and the compensated point, which is critical for system performance.

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Another disadvantage is the conduction loss of source separation switch, which conducts the load current continuously in the normal state.

The major part of the compensation delay is the detection delay for the voltage sag or interruption [5], [6]. Instantaneous detection is a rapid way to detect the voltage sag or interruption, but it is not applicable for the distorted input voltage. RMS de-tection is an accurate way to detect the voltage interruption, but it takes a longer delay time to calculate the rms value [7], [8].

This paper proposes a hybrid structure of the fast sag detec-tion algorithm for the line-interactive single-phase DVR. Also, a new switching scheme for the load separation switch is proposed to offer reliable system operation. The verification of the proposed algorithm was carried out through computer simula-tions. And the hardware implementation was confirmed by ex-perimental works with a prototype of a 3-kVA rating.

II. PROPOSED DETECTION ALGORITHM

This paper proposes a novel sag detection algorithm which has a hybrid structure composed of the instantaneous detector and the rms variation detector. According to the proposed algorithm, the rms variation detector only starts to operate when the instantaneous sag is detected.

A. Instantaneous Sag Detector

The waveform of the single-phase voltage can be expressed by the following equation, considering the harmonic compo-nents:

$$v(t) = \sum_{n=1}^{N} V_n \sin(n\omega t + \theta_n) \qquad (1)$$

where the value of n is equal to 1 if the voltage is composed of only the fundamental components. Otherwise, the value of n is an integer that is larger than 1.

If the source voltage is sinusoidal, the sag or interruption can be rapidly detected by checking the instantaneous value it-self. However, the real source voltage contains harmonic com-ponents, which brings about difficulty to detect the sag or in-terruption. The rms value detection was proposed to solve this

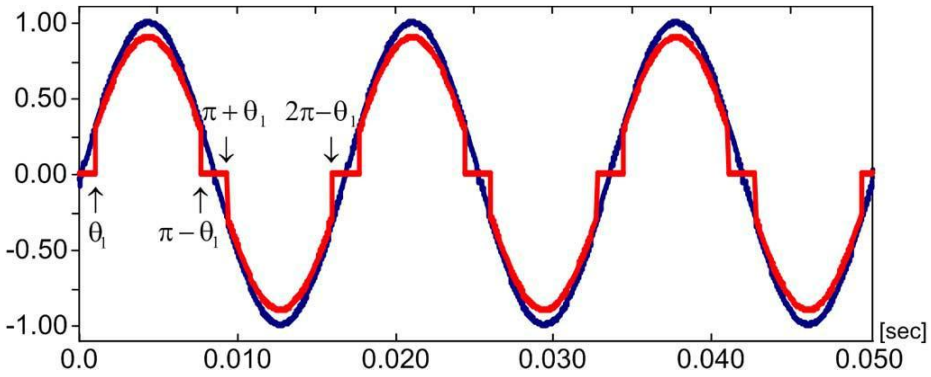

Fig. 1. Principle of instantaneous sag detection.

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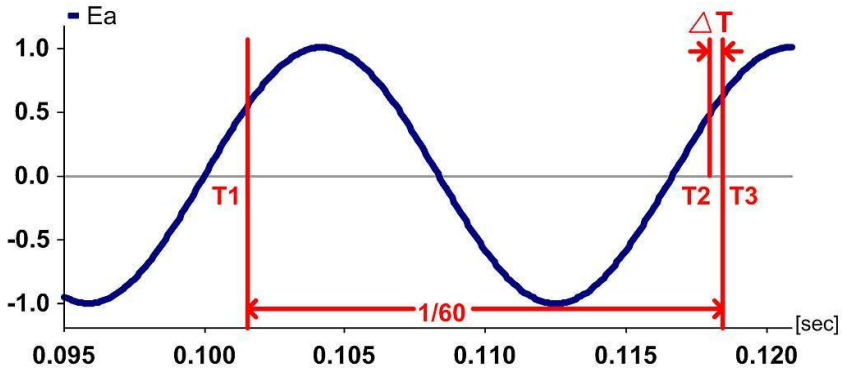

Fig. 2. Timing diagram for the calculation of rms variation criterion.

weak point. However, this method causes a longer delay time in detection because it takes time to compute the rms value from the instantaneous value.

The measured input voltage is converted into a signal with unity magnitude, dividing it with the nominal peak value as the following equation:

$$v_{\mathrm{pu}} = v(t)/v_{\mathrm{peak}}. \qquad (2)$$

Normally, the input voltage has distortion. So this voltage is converted into a unit sine signal passing through the PLL circuit

[9]. This unit sine signal is used for the generation of a reference signal in the instantaneous sag detection. The reference signal has 90% of the unit sine signal around the peak point, and zero value around the zero-crossing point as shown in Fig. 1. The reference magnitude of 0.9 was chosen, considering the sag definition in IEEE standard 1159. The instantaneous detection near the zero-crossing point is meaningless, because the sine value is too small to distinguish the sag. Considering this fact, the cut-in and cut-out angle $\pm\theta_1$ was determined by $\pm 24.5^{\circ}$ .The reference signal for instantaneous detection v_{saref} can be expressed by

$$v_{\mathrm{sag\_ref}} = \begin{cases} 0.9 \times \sin \omega t & , \theta_1 \le \theta \le \pi - \theta_1 \\ 0 & , -\theta_1 < \theta < \theta_1 \end{cases}. \qquad (3)$$

The input voltage is compared with the reference signal de-fined in (3). When the input voltage is lower than the reference, the instantaneous sag is recognized, although it is actually not. So, once the instantaneous sag is detected, the rms variation detector starts to operate for checking whether the sag is real or not.

B. RMS Variation Detector

In this proposed algorithm, the rms variation of input voltage is measured to judge the voltage sag. And a discrete Fourier transform (DFT) algorithm is used to calculate the rms value of the fundamental component. The source voltage $v(t)$ can be expressed as the following equation using the Fourier series:

$$v(t) = \frac{a_0}{2} + \sum_{n=0}^{\infty} a_n \cos n\omega_0 t + \sum_{n=0}^{\infty} b_n \sin n\omega_0 t. \qquad (4)$$

The fundamental component for $n=1$ is obtained as in (5) and (6), separating the real part and imaginary part

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$$a_1 = \frac{2}{T}\int_0^T v(t)\cos\omega_0 t\,dt \qquad (5)$$

$$b_1 = \frac{2}{T}\int_0^T v(t)\sin\omega_0 t\,dt. \qquad (6)$$

Applying the DFT for (5) and (6), (7) and (8) are obtained

$$a_1 = \frac{\sqrt{2}}{N}\sum_{i=0}^{N} v\left(t - i\frac{T}{N}\right)\cos\left(2\pi\frac{i}{N}\right) \qquad (7)$$

$$b_1 = \frac{\sqrt{2}}{N}\sum_{i=0}^{N} v\left(t - i\frac{T}{N}\right)\sin\left(2\pi\frac{i}{N}\right). \qquad (8)$$

Using the value of a_1 and b_1, the rms value of the fundamental component can be easily obtained as the following:

$$V_{\mathrm{RMS}} = \sqrt{a_1^2 + b_1^2}. \qquad (9)$$

The determination of criterion value for the rms variation detector was carried out by using the following procedure.

If the voltage sag occurred at $T2$ and the allowable detection time is at $T3$, the criterion value ΔE is calculated by subtracting the rms value at $T2 V_{\mathrm{rms}T2}$ from the rms value at $T3 V_{\mathrm{rms}T3}$.

The allowable detection time $\Delta T = T3\_T2$ is determined by considering the sampling period and the number of samplings.

The value of ΔT is 1.667 ms if the sampling period and the number of sampling are assumed to be 98 μs and 17where T is the period of power frequency, k is the sag level which was determined to be 0.9 by the definition of voltage sag in IEEE standard 1159.

Equation (10), shown at the bottom of the page, can be rear-ranged by the following equation using the trigonometric rule, as shown in (11) at the bottom of the next page.

$$V_{\mathrm{rms},T_3} = \sqrt{\frac{1}{T}\left\{\int_{T_1}^{T_2}\left(\sqrt{2}V_{\mathrm{rms},\,T_2}\sin\omega t\right)^2 dt + \int_{T_2}^{T_3}\left(\sqrt{2}\,kV_{\mathrm{rms},\,T_2}\sin\omega t\right)^2 dt\right\}} \qquad (10)$$

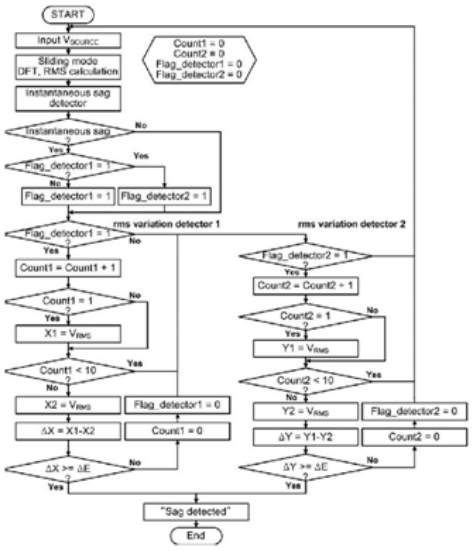

Fig. 3.Hybrid detection method for voltage interruption.

Therefore, the criterion value ΔE can be defined by the fol-lowing equation:

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$$\Delta E = V_{\mathrm{rms},T_2} - V_{\mathrm{rms},T_3}. \quad (12)$$

In (12), it is confirmed that the value of ΔE changes ac-cording to the instant of sag occurrence.

Fig. 3 shows the software structure of the hybrid detection method which consists of an instantaneous detector, the rms variation detector-1, and the rms variation detector-2. The source voltage passes through the sliding-window DFT, the rms calculation procedure, and the instantaneous sag detector. If instantaneous sag is detected, the rms variation detector-1 is selected and the present rms value is stored at$X1$. While the instantaneous sag is effective, the same procedure continues for 17 times. It takes 1.667 ms because the control period is μs. The final rms value is stored at $X2$ to calculate the rms variation ΔX=$X2$_$X1$. If the rms variation ΔX is larger than ΔE, the sag is acknowledged. Otherwise, the next input is processed continuously.

If the instantaneous sag occurs while the rms variation de-tector-1 is under operation, it is impossible to calculate the rms variation within allowable time. So, the rms detector-1 cannot successfully detect the actual sag. In order to remove this weak point, the rms variation detector-2 starts to operate at this mo-ment. Therefore, two state machines of the rms variation de-tector operate in parallel with the complementary role.

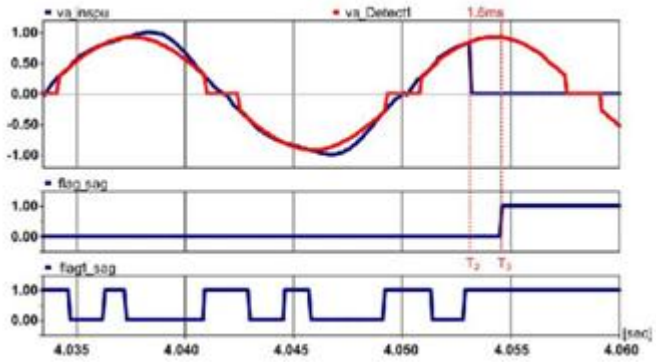

Fig. 4. Instantaneous detection scheme for input voltage.

Fig. 4 shows a simulation result obtained from the proposed sag detection algorithm when the source voltage has 5% of third harmonics and 3.5% of fifth harmonics. The instantaneous sag is detected every time when the input voltage is lower than the reference signal as shown in the third graph. But the real sag that is detected by the rms variation detector is shown in the second graph. It is confirmed that there is no real sag for the first cycle. According to the first and second graphs, it is known that the detection delay is about 1.6 ms.

Fig. 5 shows the performance comparison result of the pro-posed detection method with that of the rms detection method, when the input source voltage has 5% of 3rd harmonics and 3.5% of 5th harmonics. The proposed method has a delay time of 1.6 ms, while the rms detection has much longer delay time at T4. In [6], the authors show a similar analysis result that is obtained by comparison of their method with the rms detection method. Their method has a delay time of 2 ms. This implies that the proposed method in this paper shows better performance than the method described in [6].

III. LINE-INTERACTIVE DVR

A. System Configuration

Fig. 6 shows a configuration of the DVR with the proposed algorithm including the source and the load. The DVR consists of an inverter, supercapacitor, power transformer, antiparallel thyristor switch, and system controller. In normal state, the source supplies power directly to the load through the thyristor switch. When the

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voltage interruption occurs, the controller de-tects the disturbance and the inverter supplies nominal voltage through the power transformer by discharging the supercapac-itor, in which the antiparallel thyristor switch turns off to separate the source.

$$V_{\text{rms},T_3} = V_{\text{rms},T_2}\sqrt{\frac{1}{T}\left\{\int_{T_1}^{T_2}(1-\cos 2\omega t)\,dt + k^2\int_{T_2}^{T_3}(1-\cos 2\omega t)\,dt\right\}}. \quad (11)$$

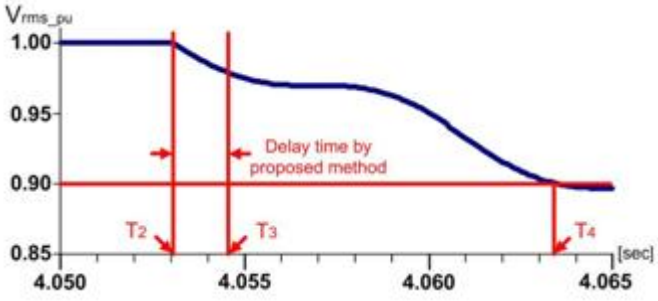

Fig. 5. Performance analysis of the proposed detection method.

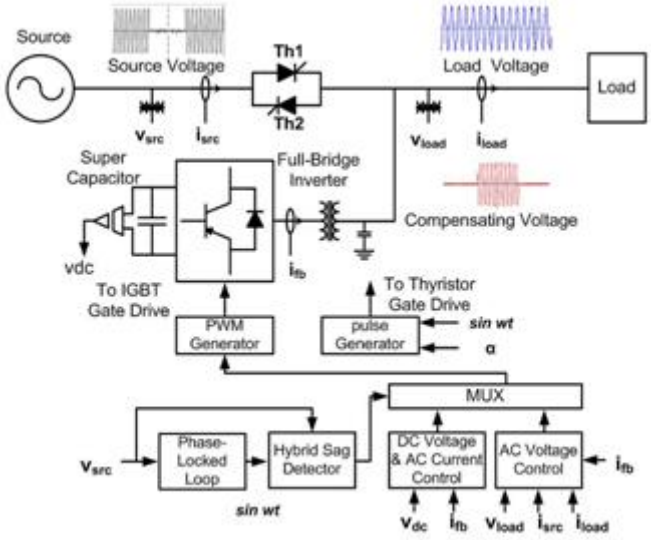

Fig. 6. Configuration of line-interactive DVR.

When the source is recovered, the compensating voltage is removed by cutting off the gate signals for the inverter. The thyristor switch turns on to supply power from the source. After elapsing a few seconds, the inverter starts charging the super capacitor to be ready for the next disturbance.

The measured source voltage is sent to the PLL to obtain the unit sine signal, which is needed to calculate the reference value for the instantaneous sag detector. DFT operation is carried out in a sliding-window pattern for a half period of power frequency. The source voltage is passed through the hybrid detection flow shown in Fig. 3. Once the sag is detected, the inverter injects a sinusoidal voltage obtained from the current and voltage-control procedures.

The dc voltage and ac current of the full-bridge inverter are sent to the dc voltage and ac current control. The load voltage and current, the source current, and the full-bridge inverter cur-rent are sent to the ac voltage control. The output of these control blocks is sent to the MUX. The output of MUX is sent to the PWM pulse generation. The unit sine from the PLL is sent to the gate pulse generator for the antiparallel thyristor switch.

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The size of the supercapacitor bank is determined depending on the duration of voltage interruption and the size of the con-nected load. It is assumed that the voltage interruption has a du-

TABLE I SPECIFICATION OF SUPERCAPACITOR

Items	Characteristics
Rated Working Voltage	2.7VDC
Operating Temperature	-40 to +60°C
Nominal Cap. Range	100F
Equivalent Series Resistance	0.014Ω (@ 1kHz)

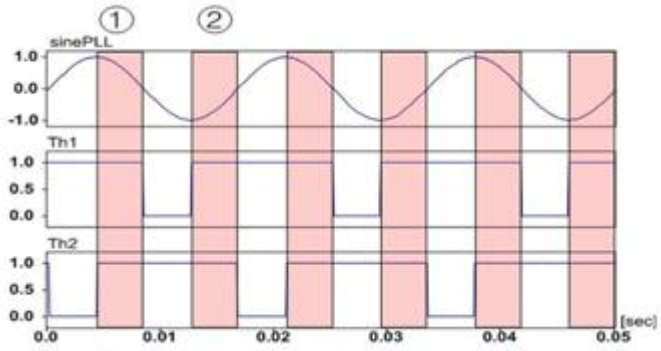

Fig. 7. Gate pulse supplying the thyristor switch.

ration of 2 s and the load has a power rating of 3 kVA. Therefore, the total energy to be released during the voltage interruption is designed to be 6 kJ. The bank of the supercapacitor is designed considering the size of energy storage, the dc-link voltage, and the voltage and current rating of each capacitor unit. Table I shows the specification of the selected supercapacitor.

The bank is designed in order to utilize the upper 25% of max-imum storage capacity, considering the expandability of opera-tion capacity. The maximum current flows through the superca-pacitor bank when it discharges the maximum power. The min-imum voltage across the supercapacitor bank can be determined with the maximum discharge power and the current rating.

It is assumed that the supercapacitor is charged by 2.43 V, which is 90% of the maximum charging voltage 2.7 V, considering 10% margin. The lowest discharge voltage is determined to be 2.1 V. Therefore, the maximum and minimum voltages of energy storage were determined by 105 V and 125 V, considering that 50 units of the supercapacitor were connected in series with enough safety margin.

B. Thyristor Switch Operation

The line-interactive DVR with the proposed algorithm has an antiparallel thyristor switch in Fig. 7. It holds on state in normal operation, and disconnects the source when the sag or interruption occurs.

If the inverter starts to compensate at the instant when the thyristor switch is on, the inverter current flows into the source side instead of the load side. The inverter supplies overcurrent and the load voltage cannot be restored because the source impedance is very small. Therefore, the inverter must start to compensate after the thyristor switch turns off by compulsion.

The gate pulse for the thyristor switch is normally supplied for 180 ₀ in case of the resistive load. But in case of inductive or capacitive load, it should be supplied for more than 180₀ . In this paper, the gate pulse was supplied for 270₀ , considering enough margin according to the load type. So the gate pulses for $Th1$ and $Th2$ are

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supplied for 1.5 π. Both gate pulses are overlapped twice for 0.5 π in every cycle as shown in Fig. 7. One band locates between 0.5 π and π, and other band locates between and 1.5 π and 2 π.

At band 1, since both gate pulses for $Th1$ and $Th2$ are in on-state, both the source voltage and the inverter voltage are positive at the instant of sag. Even though both gate pulses are re-moved after detecting the sag, $Th1$ turns off and $Th2$ holds the conduction state on the contrary. This causes the reverse current flow. In order to prevent the reverse current, the system detects the load current and makes both thyristor switches turn off.

At band 2, since both gate pulses for $Th1$ and $Th2$ are in on-state, both the source voltage and the inverter voltage are negative at the instant of sag. Even though both gate pulses are removed after detecting the sag, $Th2$ turns off and $Th1$ holds the conduction state. This causes the reverse current flow. In order to prevent the reverse current, the system detects the load cur-rent and makes both thyristor switches turn off.

When the voltage sag occurs, the inverter injects a voltage after the control turns off the thyristor switch by checking the phase angle of source voltage and that of source current.

$$v_{\text{inv}} = v_{\text{src}} K_T + L \frac{I_{\text{src}}}{K_T T} \qquad (13)$$

The turnoff time of the thyristor switch is determined by di-viding the source voltage by the minimum inverter voltage. The thyristor switch is turned off considering the voltage difference due to the transformer characteristic.

C. Inverter Output Voltage Control

When the sag or interruption occurs, the full-bridge inverter supplies the nominal voltage to the load after preventing the re-verse current flow. Fig. 8 shows a voltage control scheme developed for the full-bridge inverter in DVR. In order to make the control simple and to suppress the output voltage distortion, an open-loop control with a feedforward path for the capacitor cur-rent was selected. The general P control for the output voltage gives rise to the steady-state error and the distortion, depending on the load characteristic. The ac capacitor is connected to the inverter output terminal for operating as an LC filter with the leakage reactance of transformer to cutoff the harmonics due to switching operation.

The general open-loop control generates the output voltage distortion because it brings about overshoot and oscillation for the step change of the inverter voltage. In order to solve this problem, the capacitor current is measured, and its differential value is added to the inverter voltage control. This method also offers rapid rise of the output voltage. However, since the mag-nitude of output voltage varies depending on the size of load, the output voltage is adjusted by calculating the effective value for one period right after the compensation is completed. This can overcome the weak point of open –loop control for the output voltage.

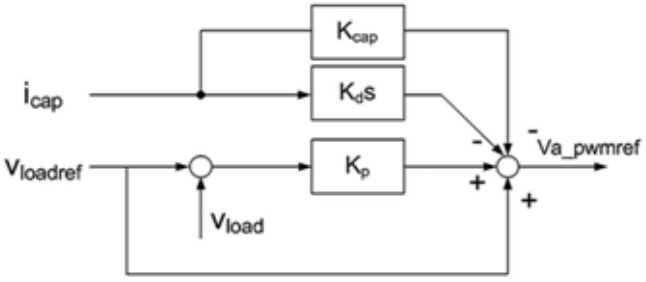

Fig. 8. Inverter output voltage control.

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Table 2. Circuit Param

Voltage Rating	220V, 60Hz
Power Rating	3kVA
Source Reactance	0.5mH
Energy Storage Capacitor	1.667F
Power Transformer	3kVA, 50:220V, 3%
IGBT switch	600V, 200A
Switching Frequency	10kHz

IV. COMPUTER SIMULATION

Many computer simulations with PSCAD/EMTDC software were carried out for analyzing the performance of the proposed DVR. The power circuit and controller were modeled as close as to the real system, using the passive and active components, and the built-in control block in PSCAD/EMTDC software. Par-ticularly, the controller was designed by using the user-defined model programmed with C language in order to implement the control action and PWM pulse generation as real as possible. It is very effective to implement the hardware controller using a digital signal processor (DSP). Table II shows the circuit pa-rameters for a 3-kVA DVR system considered in the simulation.

Fig. 9(a) shows the source voltage, the load voltage, and the compensating current from the inverter when 50% voltage sag occurs. The load voltage maintains a constant value because the inverter injects a nominal voltage during the sag.

Fig. 9(b) shows the expanded waveform focused on the sag beginning point. The load voltage is restored within 2.0 ms after the instant when the voltage sag occurs. This delay is due to the sag detection time and the turnoff time of the thyristor switch.

Fig. 10(a) shows the source voltage, the load voltage, and the compensating current from the inverter when the voltage interruption occurs. The load voltage maintains a constant value be-cause the inverter injects a nominal voltage during the interruption.

Fig. 10(b) shows the expanded waveform focused on the interruption beginning point. The load voltage is restored within 2.0 ms after the instant when the voltage interruption occurs. This delay is due to the interruption detection time and the turnoff time of the thyristor switch.

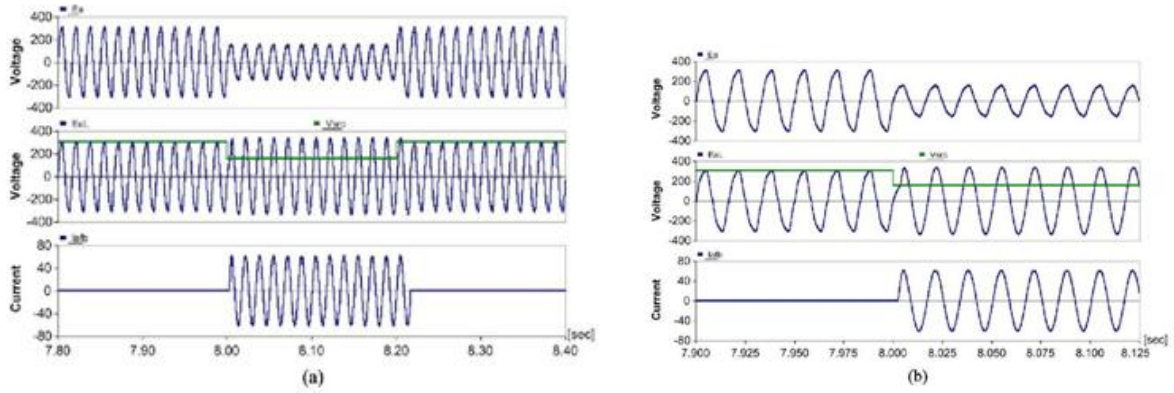

Fig. 9. Simulation results for voltage sag. (a) Source voltage, load voltage, compensating current. (b) Expanded waveform at the interruption beginning point.

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V. PROTOTYPE EXPERIMENT

A 3-kVA prototype DVR was built and tested to confirm the feasibility of hardware implementation, based on the simulation results. The prototype is composed of a full-bridge inverter, gate-drive circuit, supercapacitor bank, power transformer, an-tiparallel thyristor switch, DSP controller, and display circuit as shown in Fig. 11. All of the circuit parameters for the hardware prototype are exactly the same as in Table II.

One remarkable feature of the proposed DVR is the fast detection and compensation, which utilizes the algorithm described in Section II. The proposed fast detection algorithm can be implemented in real-time operation using the high-performance DSP controller. The DSP controller offers a display function, which monitors the whole system operation and indicates the number of voltage disturbances in real time.

The DSP controller was designed by using the TMS320vc33 DSP chip for real-time operation and the EPLD chip for logic implementation. The developed DVR prototype sets the operation frequency automatically by checking the source voltage when the system starts up. All operation is carried out automatically when the main switch is turned on.

Fig. 12(a) shows the source voltage, the load voltage, and the compensating current from the inverter when 50% voltage sag occurs. The load voltage maintains a constant value as con-firmed in the simulation results. Fig. 12(b) shows the expanded waveform focused on the sag beginning point. The load voltage

is restored within 2.0 ms as confirmed in the simulation results. This delay is due to the sag detection time and the turnoff time of the thyristor switch.

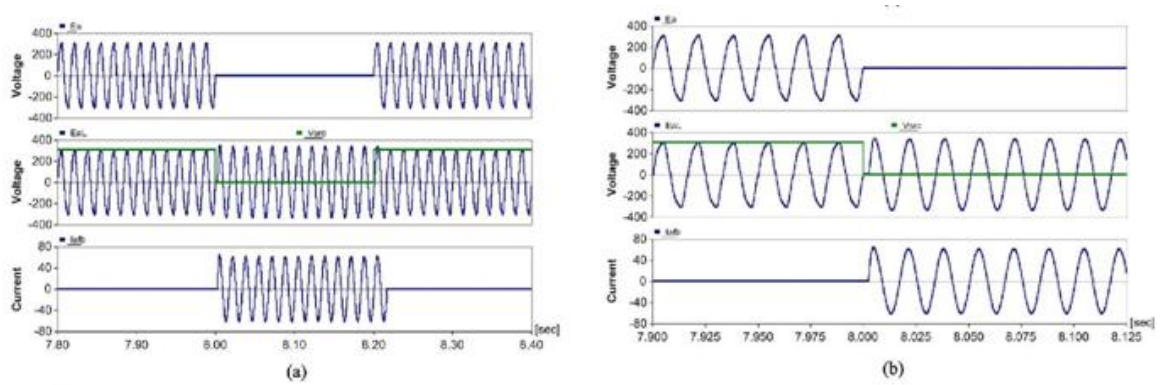

Fig. 10. Simulation results for voltage interruption. (a) Source voltage, load voltage, compensating current. (b) Expanded waveform at the interruption be-ginning point.

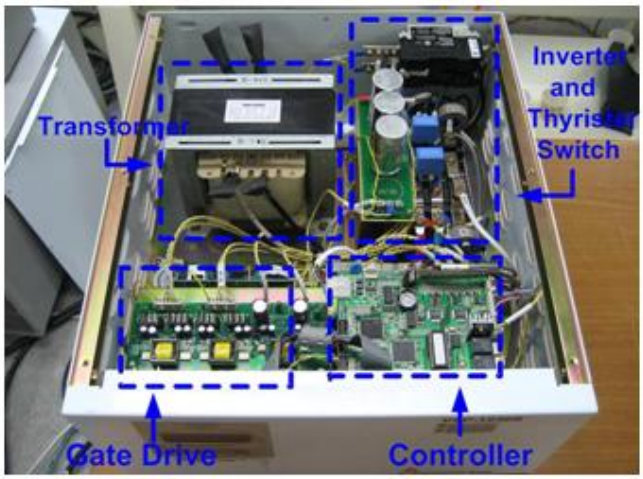

Fig. 11. Prototype of the line-interactive DVR with the proposed algorithm.

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Fig. 13(a) shows the source voltage, the load voltage, and the compensating current from the inverter when voltage interrup-tion occurs. The load voltage maintains a constant value as con-firmed in the simulation results. Fig. 13(b) shows the expanded waveform focused on the interruption beginning point. The load voltage is restored within 2.0 ms as confirmed in the simulation results. This delay is due to the sag detection time and the turnoff time of the thyristor switch.

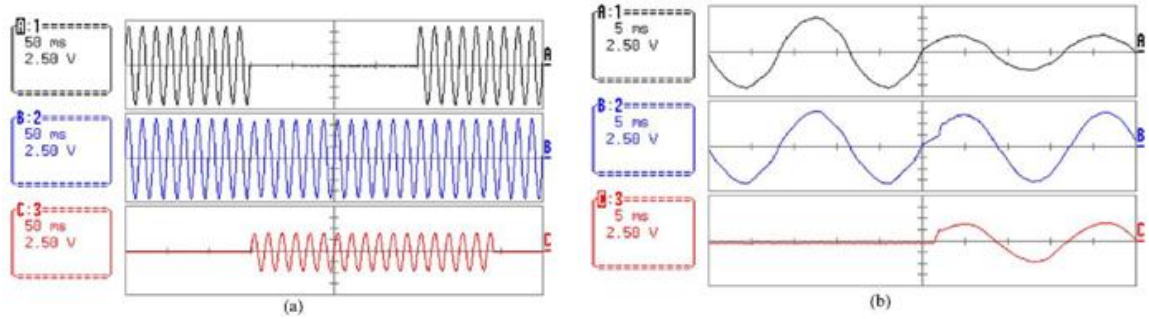

Fig. 12. Experimental results for voltage sag. (a) Source voltage, load voltage, compensating current. (b) Expanded waveform at the sag beginning point.

Through the experimental results, it is confirmed that the DVR with the proposed algorithm can restore the input voltage within 2.0 ms from the instant when the source disturbance occurs.

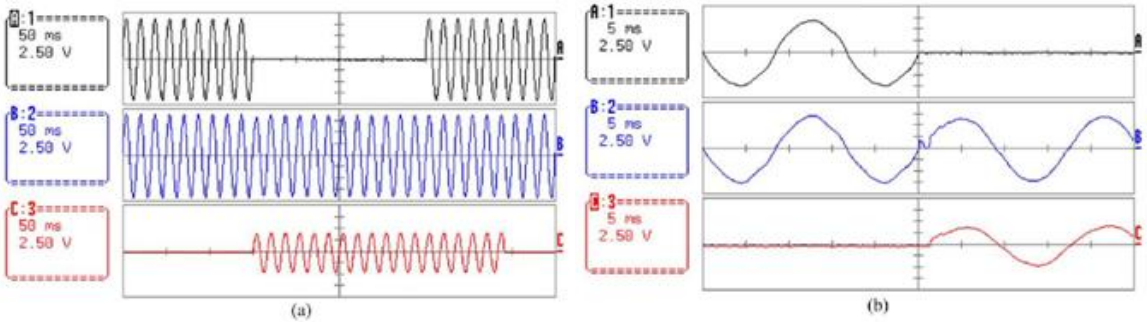

Fig. 13. Experimental results for voltage interruption. (a) Source voltage, load voltage, compensating current. (b) Expanded waveform at the sag beginning point.

VI. CONCLUSION

The proposed detection algorithm has a hybrid structure com-posed of an instantaneous sag detector and the rms variation de-tector. The source voltage passes through the instantaneous sag detector part. If instantaneous sag is detected, the rms variation detector-1 is selected to calculate the rms variation. The rms variation detector-2 is selected when the instantaneous sag oc-curs during the operation of the rms variation detector-1.

The feasibility of the proposed detection algorithm was verified through computer simulations and experimental works with a 3-kVA hardware prototype. The line-interactive DVR with the proposed algorithm can compensate the input voltage sag or interruption within 2.0-ms delay.

The DVR with the proposed detection algorithm can effec-tively compensate the voltage interruption in the sensitive loads, such as a computer, automation device, and communication de-vice.

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