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AN IMPROVED HYBRID DSTATCOM TOPOLOGY TO COMPENSATE REACTIVE AND NON LINEAR LOADS

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ABSTRACT

Traditionally, static capacitors and passive filters have been utilized to improve power quality (PQ) in a distribution system. However, these usually have problems such as fixed compensation, system-parameter-dependent performance, and possible resonance with line reactance. A distribution static compensator (DSTATCOM) has been proposed in the literature to overcome these drawbacks. It injects reactive and harmonics component of load currents to make source currents balanced, sinusoidal, and in phase with the load voltages. However, a traditional DSTATCOM requires a high-power-rating voltage source inverter (VSI) for load compensation. The power rating of the DSTATCOM is directly proportional to the current to be compensated and the dc-link voltage. Generally, the dc-link voltage is maintained at much higher value than the maximum value of the phase-to-neutral voltage in a three-phase four-wire system for satisfactory compensation (in a three-phase three-wire system, it is higher than the phase-to-phase voltage). However, a higher dc-link voltage increases the rating of the VSI, makes the VSI heavy, and results in higher voltage rating of IGBT switches. It leads to the increase in the cost, size, weight, and power rating of the VSI.

Keywords - Distribution static compensator (DSTATCOM), hybrid topology, passive filter, power quality (PQ).

I. INTRODUCTION

PQ problems are not solved completely due to uncontrollable reactive power compensation and high costs of new feeders and UPS. Conventionally, Static VAR Compensators (SVCs) have been used in conjunction with passive filters at the distribution level for reactive power compensation and mitigation of the power quality problem. Though SVCs are very effective system controllers used to provide reactive power compensation at the transmission level, their limited bandwidth, higher passive element count that increases size and losses, and slower response make them unsuitable for the modern day distribution requirement. Another compensating system has been proposed by employing a combination of SVC and active power filter, which can compensate three phase loads in a minimum of two cycles. Thus, a controller which continuously monitors the load voltages and currents to determine the right amount of compensation required by the system and the less response time should be a viable alternative. Distribution Static Compensator (DSTATCOM) has the capacity to overcome the above drawbacks by providing precise control and fast response during transient and steady state, with reduced foot print and weight. The DSTATCOM has emerged as a promising device to provide solution not only for voltage related issues but a host of other current related power quality problem’s solutions such as voltage regulation , load balancing , reactive power compensation , power factor correction & improvement and current harmonic control. This project aims at presenting a comprehensive review of DSTATCOM for power quality improvement on distribution system. This project covers the different configurations used, the control methodologies, and their selection for specific applications.

II. PROPOSED DSTATCOM TOPOLOGY

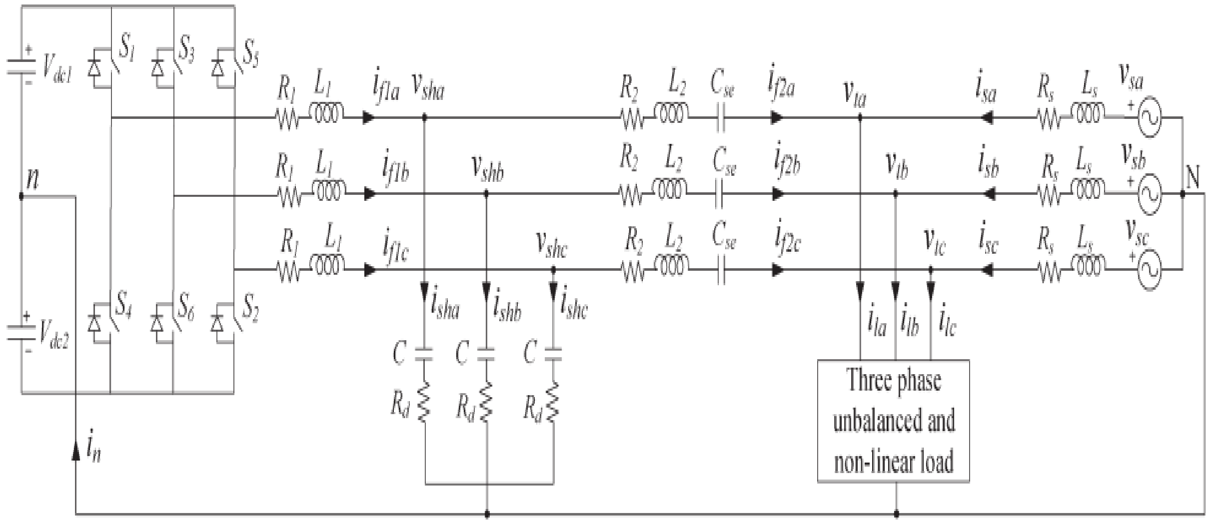

Fig.1 Proposed DSTATCOM topology to compensate unbalanced and nonlinear loads

The proposed DSTATCOM three-phase equivalent circuit diagram is shown in fig.1. It is realized by using three-phase four-wire two-level neutral-point-clamped VSI. An LCL filter is connected at the front end of voltage source inverter with series capacitance. This LCL filter reduces the size of the passive components reHere $R_1$and L_1 represent resistance and inductance at VSI side; and represents inductance and resistance at load end side of the system. C is filter capacitance which forms LCL filter in all three phases. $R_d$is damping resistance used in series with the capacitance C, provides passive damping of the overall system and damp out the resonance. Here $i_{f1a}$and i_{f2a} are filter currents in phase-a and similar in all three phases. $V_{sha}$is voltage across LCL filter and i_{sha} is current through LCL filter, this is similar for other two phases. The voltage across the DClink capacitors are maintained constant i.e. V_{dc1}=V_{dc2}=V_{dcref}. The source and load of DSTATCOM are connected to a common point called point of common coupling (PCC).

III. DSTATCOM CONTROL

The control block diagram of DSTATCOM is shown in Fig.2. The DSTATCOM is controlled in such a way that the source currents are balanced, sinusoidal, and in phase with the respective terminal voltages. In addition, average load power and losses in the VSI are supplied by the source. Since the source considered here is non stiff, the direct use of terminal voltages to calculate reference filter currents will not provide satisfactory compensation Therefore, the fundamental positive sequence components of three-phase voltages are extracted to generate reference filter currents (*i*∗f2a, *i*∗f2b, and *i*∗f2c) based on the instantaneous symmetrical component theory. These currents are given as follows:

$$\mathbf{i}^*_{f2a} = \mathbf{i}_{1a} - \mathbf{i}^*_{sa} = \frac{\mathbf{v}^+_{ta1}}{\Delta^+_1}(\mathbf{P}_{1avg} + \mathbf{P}_{loss}) \qquad \mathbf{(1)}$$

$$\mathbf{i}^*_{f2b} = \mathbf{i}_{1b} - \mathbf{i}^*_{sb} = \frac{\mathbf{v}^+_{tb1}}{\Delta^+_1}(\mathbf{P}_{1avg} + \mathbf{P}_{loss}) \qquad \mathbf{(2)}$$

$$\mathbf{i}^*_{f2c} = \mathbf{i}_{1c} - \mathbf{i}^*_{sc} = \frac{\mathbf{v}^+_{tc1}}{\Delta^+_1}(\mathbf{P}_{1avg} + \mathbf{P}_{loss}) \qquad \mathbf{(3)}$$

Where v^+_{ta1}, v^+_{tb1}, v^+_{tc1} are fundamental positive sequence voltages at the respective phase load terminal, and $\Delta^+_1 = (v^+_{ta1})^2 + (v^+_{tb1})^2 + (v^+_{tc1})^2$. The terms$P_{lavg}$ andP_{loss} represent the average load power and the total losses in the VSI, respectively. The average load power is calculated using a moving average filter for better performance during transients and can have a window width of half-cycle or full cycle depending upon the odd or odd and even harmonics, respectively, present in the load currents. At any arbitrary time *t*1, it is computed as,

$$\mathbf{P}_{lavg} = \frac{1}{T}\int_{t1-T}^{t1}(\mathbf{v}_{ta}\,\mathbf{i}_{la} + \mathbf{v}_{tb}\,\mathbf{i}_{lb} + \mathbf{v}_{tc}\,\mathbf{i}_{lc})\mathbf{dt}\mathbf{(4)}$$

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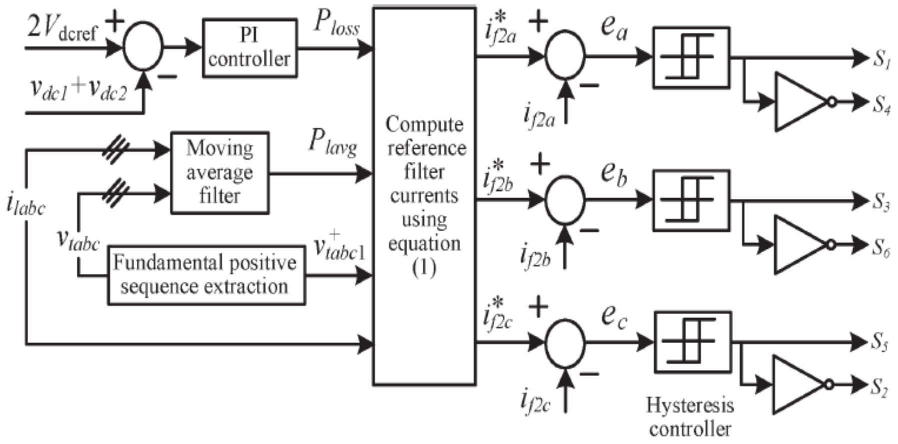

Fig.2 Control Diagram of DSTATCOM

The total losses in the VSI are computed using a proportional–integral (PI) controller at the positive zero crossing of phase-*a* voltage. It helps in maintaining the dc-link voltage $V_{dc1} + V_{dc2}$ at a reference value $2V_{dcref}$ by drawing a set of balanced currents from the source and is given as,

$$\mathbf{P}_{loss} = \mathbf{K}_p\,\mathbf{e}_{vdc} + \mathbf{K}_i\int \mathbf{e}_{vdc}\mathbf{dt} \qquad \mathbf{(5)}$$

Where K_p, K_i, $e_{vdc}$are the proportional gain, integral gain, and voltage error of the PI controller, respectively.

IV. DESIGN OF LCL FILTER PARAMETERS

While designing suitable values of LCL filter components, constraints such as cost of inductor, resonance frequency f_{res}, choice of damping resistor Rd, and attenuation at switch,frequency f_{sw} should be consider.

Consider only L1 of the passive filter, as shown in Fig.1, is used. The value of inductance L1 is chosen from a tradeoff, which provides a reasonably high switching frequency and a sufficient rate of change of the filter current, such that the VSI currents follow the reference currents. At any point of time, the following equation represents the inductor dynamics:

$$L_1 di_{f1} = -v_t - R_1 i_{f1} + V_{dref} \tag{6}$$

For further analysis, R1 can be neglected. The inductor is designed to provide good tracking performance at maximum switching frequency, which is achieved at zero supply voltage in the HCC. Taking these into consideration, inductance L1 is given by

$$L_1 = \frac{V_{dref}}{(2h_a)(2f_{max})} = \frac{V_{dref}}{4h_a f_{max}} \tag{7}$$

where $2h_a$ is allowable ripple in the current, and fmax is the maximum switching frequency achieved by the HCC. The large ripple current will lower the IGBT switching frequency and lowers the losses. However, it can be seen that the smaller ripple current results in higher inductance and, thus, more core losses. Therefore, a ripple current of 20% is taken while compromising the ripple and inductor size. The use of a series capacitor has reduced the dc-link voltage to 200 V.

Once $L_1$is chose to attenuate lower order harmonics, $L_2$and C need to be designed for elimination of higher order harmonics. At higher frequencies, the impedance offered by C_{se} will be much lower than that of L_2 and can be neglected while designing LCL filter parameters. Neglecting the values of R_1, R_2, and C_{se} at higher frequencies, the following transfer functions are obtained,

$$\frac{i_{f1}(s)}{V_{inv}(s)} = \frac{s^2 + \frac{1}{L_2 C}}{sL_1\left(s^2 + \left(\frac{L_1+L_2}{L_1 L_2 C}\right)\right)} \tag{8}$$

$$\frac{i_{f2}(s)}{V_{inv}(s)} = \frac{\frac{1}{L_1 L_2 C}}{s\left(s^2 + \left(\frac{L_1+L_2}{L_1 L_2 C}\right)\right)} \tag{9}$$

The expression for resonance frequency is,

$$f_{res} = \sqrt{\frac{1+K}{KL_1 C}} \tag{10}$$

Where k = L2/L1. The resonance frequency must be greater than the highest order harmonic of the current to be compensated. Usually, the magnitude of the lower order harmonics in the LCL filter is used to be more as compared with the higher order harmonics. Hence, the current through the shunt capacitor and the inductor L1 will increase for k>1. This will increase the damping power losses, the reactive power loss in inductor L1, and the inverter current. Moreover, the source current will also increase as the damping power losses are extracted from the source. Hence, L2 > L1 will result in more losses and cost. Therefore, to ensure low loss and high efficiency, a lower value of k is selected (k < 1). The capacitive reactance at resonance will be,

$$X_{cres} = \frac{1}{2\pi f_{res} C} \tag{11}$$

The power losses in the damping resistor will be,

$$P_{loss} = 3 \times R_d \times \sum_{h=1}^{n} I_{sh}^2 \qquad (12)$$

V. SIMULATION AND RESULT

The combined model of DSTATCOM and LCL filter is improved hybrid DSTATCOM. Here the simulation of Improved Hybrid DSTATCOM is carried out under reactive and nonlinear load. The simulation diagram of DSTATCOM is shown below in fig.3.

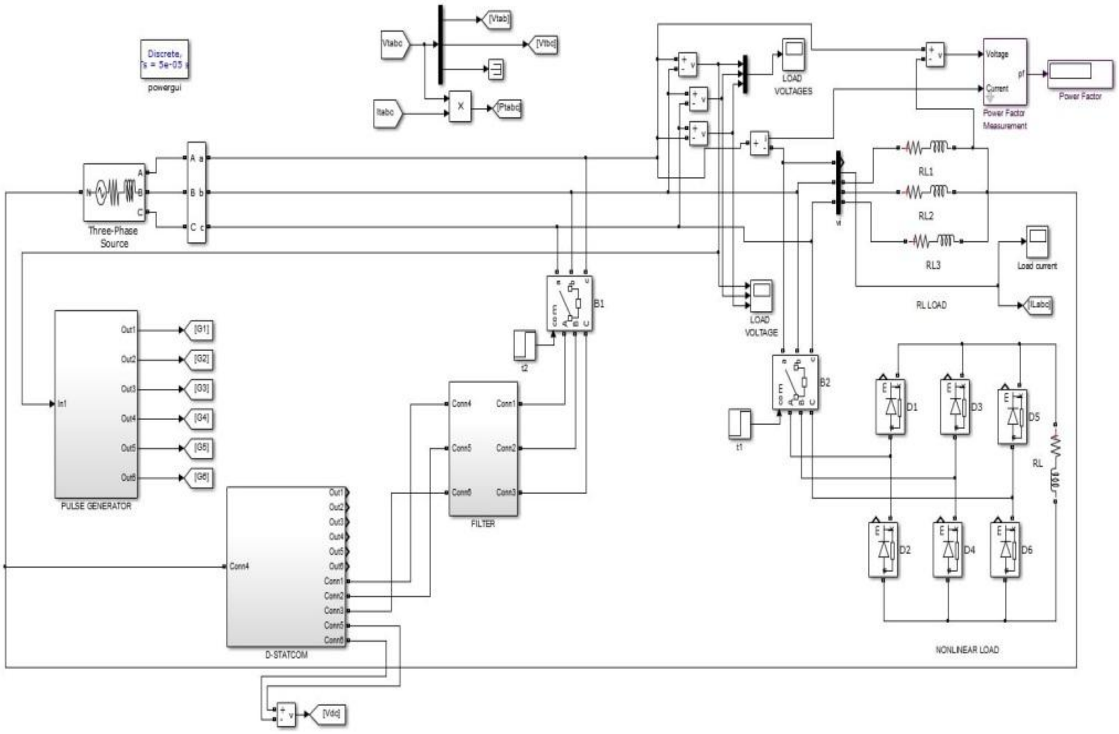

Fig.3 Simulation diagram of improved hybrid DSTATCOM

The system parameters are given in table1,

TABLE 1: Simulation parameters for Improved Hybrid DSTATCOM

System quantities	Values
Source voltage	230V Line to Neutral, 50Hz
Feeder impedance	Z_s = 1+j3.141Ω
Linear load	Z_1= 45+j0.1 Ω Z_2= 45+j0.1 Ω Z_3= 45+j0.1 Ω
RL type non linear load	Three phase full bridge rectifier with RL load of 13.5Ω, 15Mh
VSI Parameters	V_{dc} = 200V, r = 20Ω, C_{dc1} = 2600μF, C_{dc2}= 2600μF

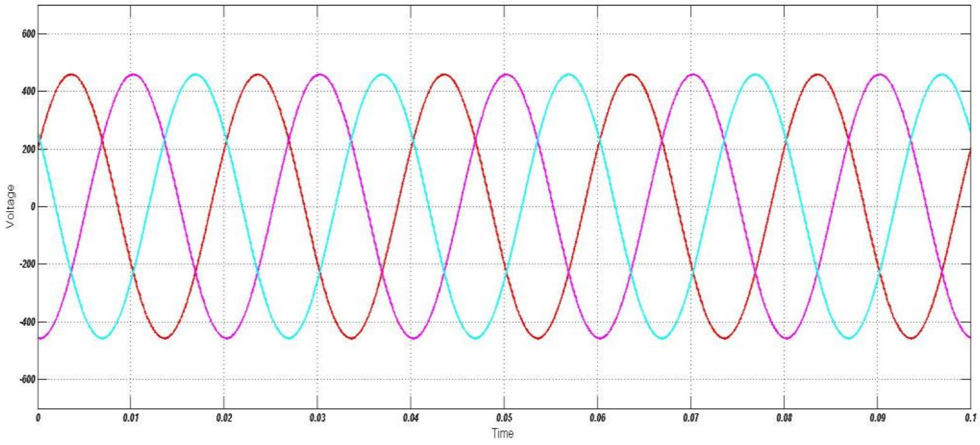

Fig.4 Three phase output voltage at load terminal

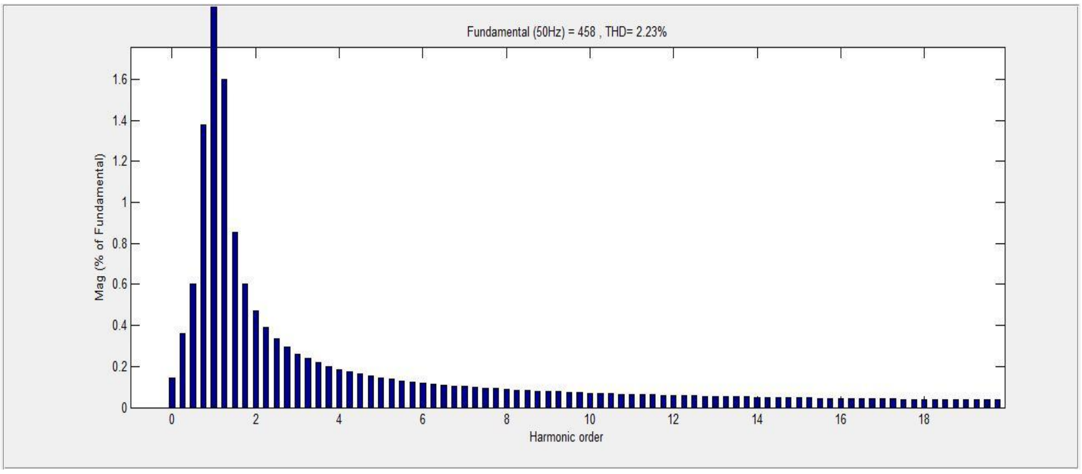

Fig.5 THD analysis of output voltage waveforms

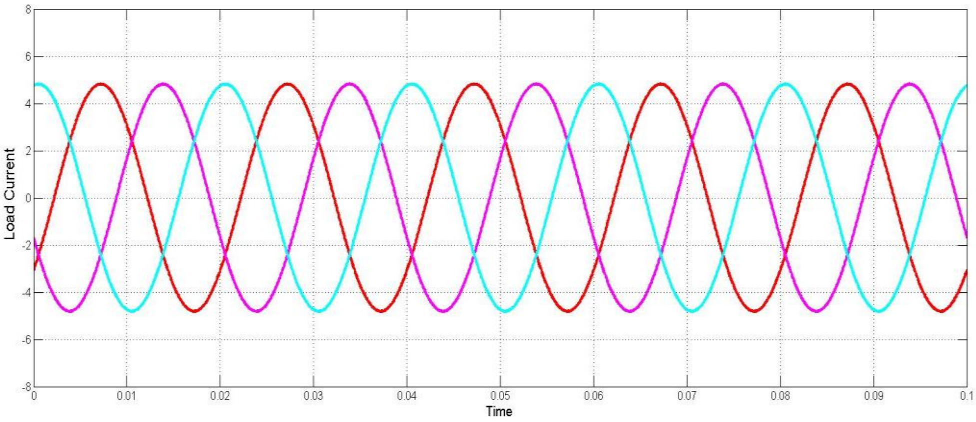

Fig.6 Three phase output current at load terminal

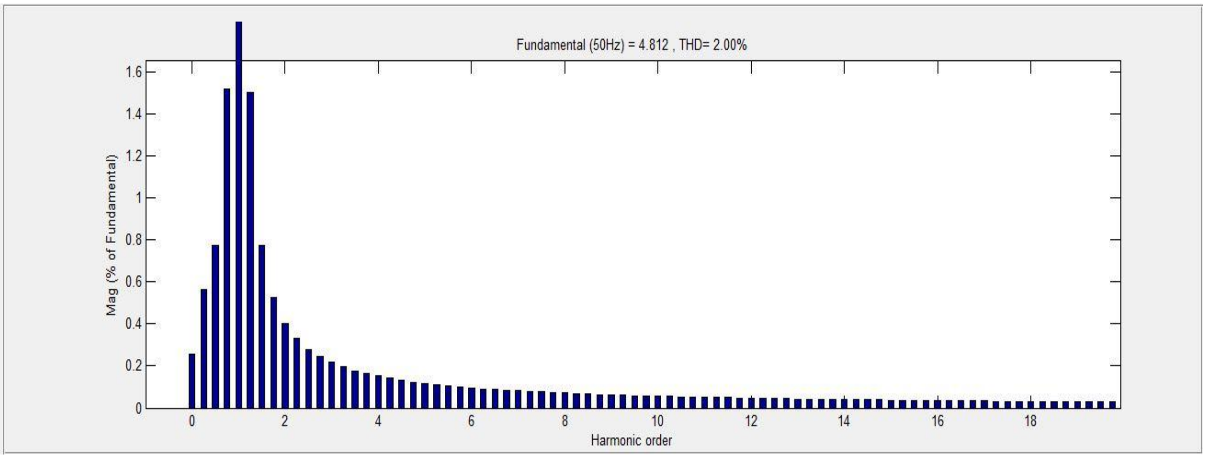

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Fig.7 THD analysis of output current waveform

VI. CONCLUSION

In this project, design and operation of an improved hybrid DSTATCOM topology is proposed to compensate reactive and harmonics (non linear) loads. The hybrid interfacing filter used here consists of an LCL filter. This topology provides improved load current compensation capabilities while using reduced dc-link voltage and interfacing filter inductance. Moreover, the current through the shunt capacitor and the damping power losses are significantly reduced compared with the LCL filter-based DSTATCOM topology. These contribute significant reduction in cost, weight, size, and power rating of the traditional DSTATCOM topology.

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