DESIGN OF LOW POWER CMOS TWO STAGE OP-AMP

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ABSTRACT

The trend towards low voltage low power silicon chip system has been growing quickly due to the increasing demand of smaller size and longer battery life for portable applications in all market. In order to as certain low power & smaller in size op-amp. CMOS op-amp is preferred. Power consumption is a critical issue in portable applications due to the limitation of the battery lifetime. The main objective of this paper is to decrease power dissipation. A CMOS two stage op-amp has been presented which operates at 1.8 v power supply using 180nm CMOS technology. The dc gain of operational amplifier is found to be 57 dB and phase margin 55 degree. Power dissipation is 1.98mw.

Keywords: CMOS Two Stage Operation Amplifier , Low Power

I INTRODUCTION

Operational amplifiers are an integral part many analog and mixed signal systems. In designing an op-amp, numerous electrical characteristics, e.g. gain bandwidth, slew rate, common mode range, output swing, offset, all have to be taken into consideration. Operational amplifier is among the most used electronic devices today, used in a wide range of consumer devices, industrial and scientific. In many applications of operational amplifiers, the gain of a single stage amplifier is not sufficient. Architectures of operational amplifiers using two or more gain stages widely used in higher gains are needed. Op-amps are available in many topologies, a two stage op-amp is an example of this kind, which is used when the high input impedance and low output impedance is needed. Power dissipation can be reduced by reducing either supply voltage or total current in the circuit or by reducing the both. As the input current is lowered though power dissipation is reduced, dynamic range is degraded. As the supply voltage decreases, it also becomes increasingly difficult to keep transistors in saturation with the voltage headroom available. Another concern that draws from supply voltage scaling is the threshold voltage of the transistor.

CMOS Op-amp can be used very efficiently for practical consequences e.g. designing of a switched capacitor filter, analog to digital converter etc. In this case the designs of the individual op amps are combined with feedback and by various parameters that affect the amplifier such as input capacitance, output resistance etc.

II BACK GROUND THEORY OF TWO STAGE OP-AMP

The topology of circuit designed is the standard CMOS two stage op-amp. It is divided into three subsection of circuit: Differential gain stage, Second gain stage, Bias string.

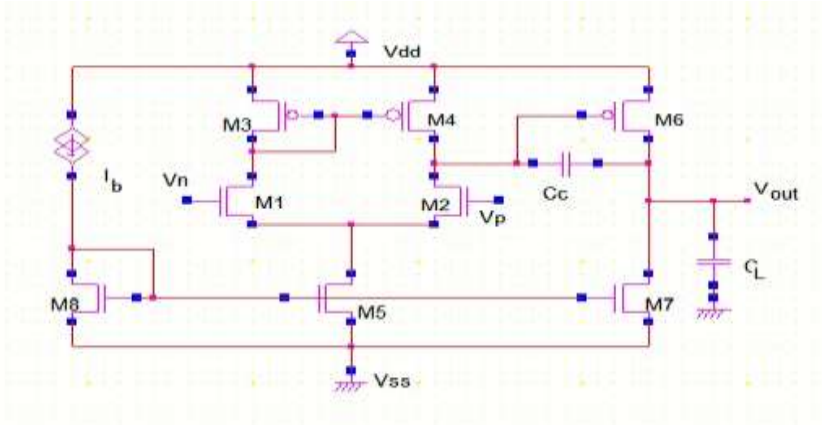

Figure 1: Schematic diagram of CMOS two stage op-amp

2.1 Differential gain stage

The first subsection of interest is the differential gain stage which is comprised of transistor M1 and M2. M1 and M2 form the basic input stage of the amplifier. The gate of M1 is the inverting input and the gate M2 is the non-inverting input. The transconductance of this stage is simply the transconductance of M1 or M2. M3 and M4 are the active load transistors of the differential amplifier. The current mirror active load used in this circuit has distinct advantage; the use of active load devices creates a large output resistance in relatively small amount of die area.

2.2 Second gain stage

The second stage is a current sink load inverter. The purpose of the second gain stage is to provide additional gain, in the amplifier. Consisting of transistor M6 and M7, this stage takes the output from the drain of M2 and amplifies it through M6 which is in the standard common source configuration. Similar to the differential gain stage, this stage employs an active device, M7, to serve as the load resistance for M6. M7 is the driver while M5 acts as load.

2.3 Bias string

The biasing of the operation amplifier is achieved with only two transistors along with a current source. Transistor M8 and the current source, supply a voltage between the gate and source of M5 and M7. Transistor M5 and M7 sink a certain amount of current based on their gate to source voltage which is controlled by the bias string.

TABLE I TARGET SPECIFICATION

Technology(nm)	180
Supply Voltage (v)	1.8
Open Loop Gain (db)	≥ 60

Gain BW(MHz)	≥ 22
PM (degree)	≥ 50
Slew Rate (v/μs)	≥ 8
CMRR (db)	≥ 40
PSRR (db)	≥ 60
Power Dissipation (mw)	≤ 1

III DESIGN STEP OF CMOS TWO STAGE OP-AMP

A design procedure assumes that the gain at dc (A_v), unity gain bandwidth (GB), input common mode range (Vin (min) & Vin (max)), load capacitance (C_L), slew rate (SR), power dissipation are given.

STEP 1: Choose the smallest device length that will keep the channel modulation parameter constant & give good matching for current mirror.

STEP 2: From the desired phase margin, choose the minimum value for Cc ; that is, for 60^0 phase margin we use the following relationship. This assumes that z ≥ 10GB.

$$C_C > (2.2/10)C_L \tag{1}$$

STEP 3: Determine the minimum value for the 'tail current' (I_5) from the largest of the two values.

$$I_5 = SR \times C_C \tag{2}$$

STEP 4: Design for S_3 from the minimum i/p voltage specification.

$$\left(\frac{W}{L}\right)_3 = \frac{I_5}{K'_P[V_{DD} - V_{in}(\max) - |V_{T03}|(\max) + V_T(\min)]^2} \tag{3}$$

STEP 5: The next step in the design is to calculate g_{m1}.

$$g_{m1} = 2\pi GB(C_C) \tag{4}$$

STEP 6: Design for S_1 to achieve the desired GB.

$$S_1 = S_2 = \frac{g_{m1}^2}{k'_N I_5} \tag{5}$$

STEP 7: Design for S_5 from the minimum i/p voltage. First calculate $V_{DS5(sat)}$ then find S_5.

$$V_{DS5} = V_{in(\min)} - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1(\max)} \geq 100mV \tag{6}$$

$$S_5 = \frac{2I_5}{k'_N (V_{DS5})^2} \tag{7}$$

STEP 8: Find S_6 & I_6.

$$g_{m6} \geq 10 g_{m1}$$

$$g_{m4} = \sqrt{2I_4 K_P S_4}, \quad I_4 = \frac{I_5}{2}$$

$$S_6 = S_4 \frac{g_{m6}}{g_{m4}} \tag{8}$$

$$I_6 = \frac{g_{m6}^2}{2k_N' S_6} \tag{9}$$

STEP 9: Design S_7 to achieve the desired current ratio between I_5 & I_6.

$$S_7 = S_5 \left(\frac{I_6}{I_5} \right) \tag{10}$$

STEP 10: Check power dissipation specification.

$$P_{diss} = (I_5 + I_6)(V_{DD} + |V_{SS}|) \tag{11}$$

TABLE III.

MOS TRANSISTOR DESIGNED FOR 180nm TECHNOLOGY

MOS Transistor	Aspect Ratio (W/L)
M1	15/1
M2	15/1
M3	3/1
M4	3/1
M5	3/1
M6	145/1
M7	65/1
M8	3/1

TABLE III. COMPARISON BETWEEN SIMULATED RESULT AND PREVIOUS PAPER RESULT

Paper	***[6]***	***[7]***	***[8]***	***[9]***	***My work***
Technology(nm)	180	180	180	180	180
Supply Voltage (v)	2.5	1.8	1.8	3	1.8
Open Loop Gain (db)	36.74	47.85	60	49.02	57
Gain BW(MHz)	16.54	-	26	-	22
PM (degree)	48.1	63	50	60.5	55
Slew Rate (v/μs)	12.5	-	-	+1.41 -1.42	-
CMRR (db)	133.69	53.68	48.7	39	-
PSRR (db)	179.38	-	-	154	-
Power Dissipation (mw)	0.804	3.58	1.3	0.039	1.98

Here "-" indicate data are not available

IV SIMULATION RESULTS

Figure 2, 3, 4 shows that the gain & phase margin & power dissipation diagram after simulation with applied at 1.8 v supply voltage on 180nm technology in T-SPICE software and gain is 57db & phase margin 55 degree. Power dissipation is 1.98mw.

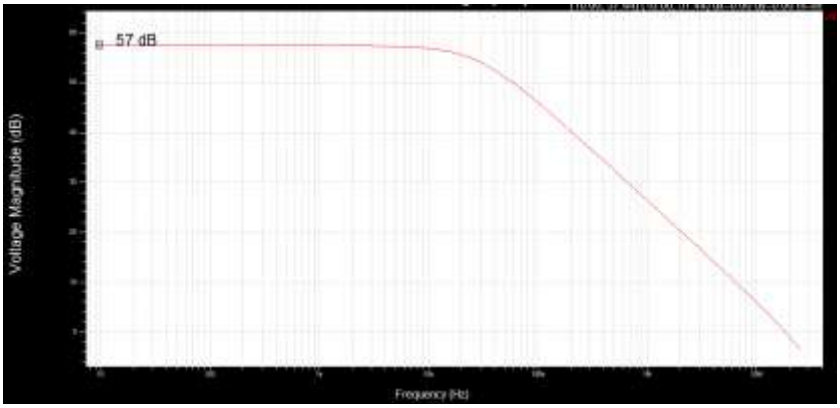

Figure 2: Gain diagram

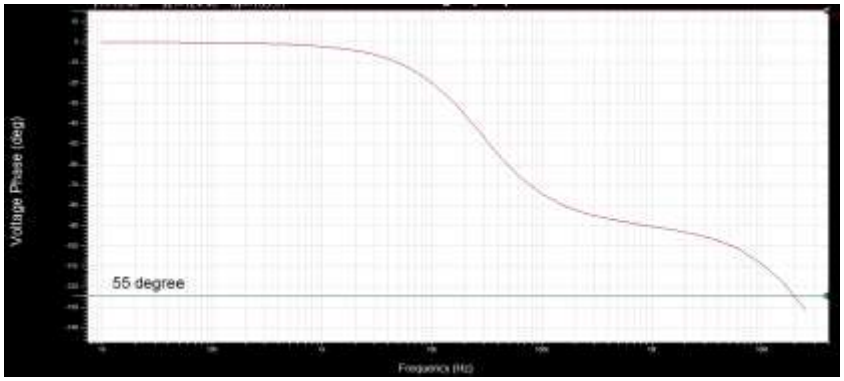

Figure 3: Phase margin diagram

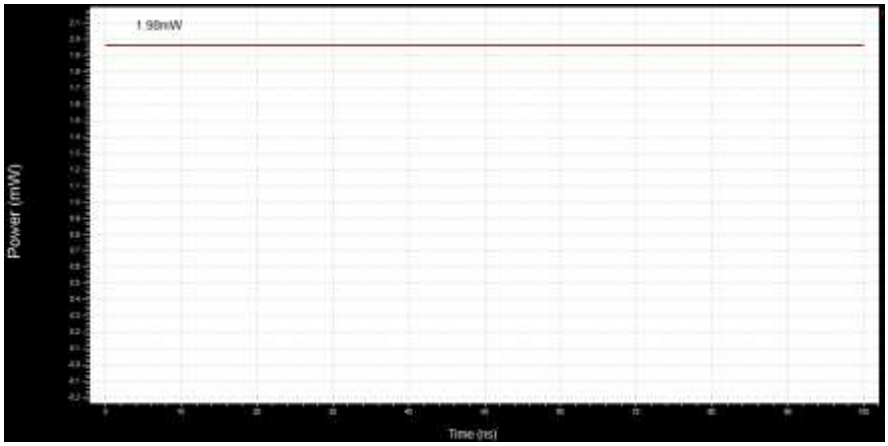

Figure 4: Power dissipation diagram

V CONCLUSION

In this paper the design of a two-stage CMOS op-amp has been presented using 180nm technology at 1.8V supply voltage. The results are simulated in T-spice (Tanner EDA) software. Circuit can be used for wide varieties of low voltage & low power application. The gain of operational amplifier is found to be 57db and phase margin 55. Power dissipation is 1.98mw.

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