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# IMPLEMENTATION OF HIGH SPEED LOW POWER DOUBLE TAIL COMPARATOR USING HSPICE

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## ABSTRACT

*Comparator is one of the basic building blocks of analog to digital converter. The need for ultra low-power, area efficient and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to improve speed and efficiency of power. In this paper, an analysis on the delay of single Tail comparator, Double Tail Comparator and double tail comparator for low power will be presented. The sub threshold leakage of transistors has usually been very small in the off state, as gate voltage is below threshold. But as voltages have been scaled down with transistor size, sub threshold leakage has become a considerable factor. Hence, to reduce the sub threshold leakage a new CMOS dynamic comparator using conventional CMOS inverter method is proposed. The circuit has a dual input single output differential amplifier which is suitable for high speed analog to digital converters with improved speed and low power dissipation. The simulation results confirm the analysis and show that in the proposed dual tail dynamic comparator both power consumption and delay time are significantly reduced even in small supply voltage. The simulation results will be shown in H-Spice.*

## I. INTRODUCTION

The clocked regenerative comparators are mostly used in High speed ADCs. Clocked comparators can make fast decisions as they have strong positive feedback in the regenerative latch. There are many analyses such as noise, offset; random decision errors and kick back noise are present. Here, a delay analysis is presented. The delay of different clocked comparators such as single tail comparator, double tail comparator and double tail comparator for low power is analyzed both theoretically and practically. For each modification in the circuit the delay and power will be reduced. The comparator design is slightly modified in order to reduce the leakage power which further reduces the total power and delay of the circuit. The simulation results show the reduction in power and delay. The delay of each comparator will be analyzed.

## II. SINGLE-TAIL COMPARATOR

This is a basic dynamic comparator which is mostly used in many Analog to Digital Converters. This topology has high input impedance, rail to rail output swing and it doesn't offer static power consumption. The circuit operates in two phases, reset phase and decision making phase depending on the clock input given. The schematic diagram of dynamic comparator is as follows,

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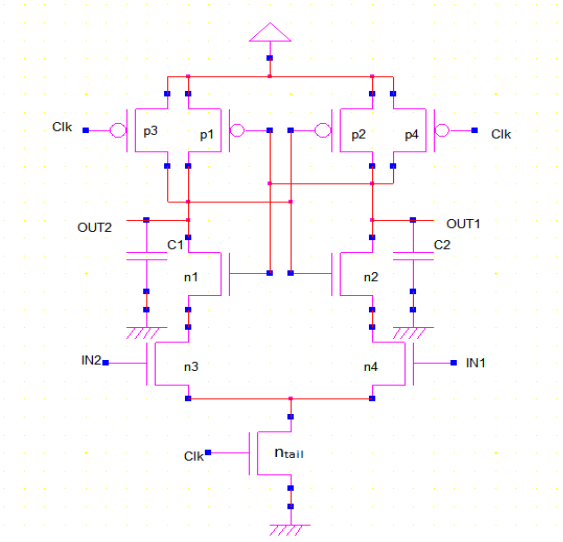


**Fig. 1 Schematic Diagram of Single Tail Comparator**

## 2.1 Operation

During reset phase, when clk=0, $n_{tail}$ is off and both the reset transistors $p_3$ and $p_4$ are on and pull both the output nodes out1 and out2 to $V_{DD}$ which indicates a start condition having a valid logic level in the reset phase. During comparison phase, when clk= $V_{DD}$, the transistors $p_3$ and $p_4$ are off, so that the out1 and out2 nodes starts discharging with different rates depending on the applied inputs $in_1$ and $in_2$. Assuming IN1>IN2, since the transistors are of same size, n4 transistor will turn on faster than n3 so that out1 discharges faster than out2. When out1 discharges down to $V_{DD}$-$|V_{thp}|$ before out2, the corresponding PMOS transistor p1 turns on pulling the other output node out2 to $V_{DD}$. Thus the latch regeneration which is caused by back to back inverters starts. Thus, Out2 will be pulled back to VDD and Out1 will be discharged to ground. If in1 < in2, the circuits works vice versa.

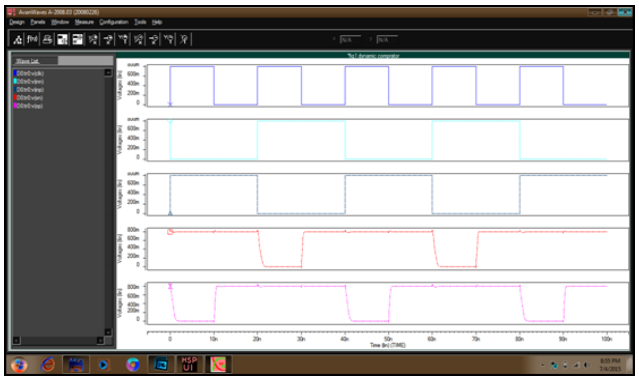

**Fig. 2 Simulated Results of Single Tail Comparator**

The expression for the delay of the single tail comparator is obtained as $t_{delay} = t_0+t_{latch}$

$$t_{delay} = 2\frac{C_L|V_{thp}|}{I_{tail}} + \frac{C_L}{g_{m,eff}}\ln\left(\frac{V_{DD}}{4|V_{thp}|\Delta V_{in}}\sqrt{\frac{I_{tail}}{\beta_{1,2}}}\right) \quad (1)$$

Simulation results specify that the effect of reducing the Vcm along with the increase of $t_0$ and reducing of $t_{latch}$ finally leads to an increase in the total delay of the comparator. This circuit structure has the advantages of high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and

mismatch. Here, parasitic capacitances of input transistors do not directly affect the output nodes' switching speed. Hence, to minimize the offset, it is possible to design large input transistors.

On the other hand, there is a disadvantage with this topology i.e., due to several stacked transistors, a sufficiently high supply voltage is needed to obtain a proper delay time. The delay time of the circuit becomes large due to lower transconductance of the latch. Another main drawback of this structure is that there is only one current path. Through the tail transistor for both the differential amplifier and the latch there is only one current path. One should prefer a small current path for the differential amplifier to keep the differential pair in weak inversion and to obtain a long integration interval. A large current path is required for the fast regeneration in the latch.

## III. DOUBLE-TAIL DYNAMIC COMPARATOR

A double-tail comparator is shown in Fig.3. Compared to previous structure, this topology has less stacking of transistors; hence, it can be operated at lower supply voltages compared to the single Tail dynamic comparator.

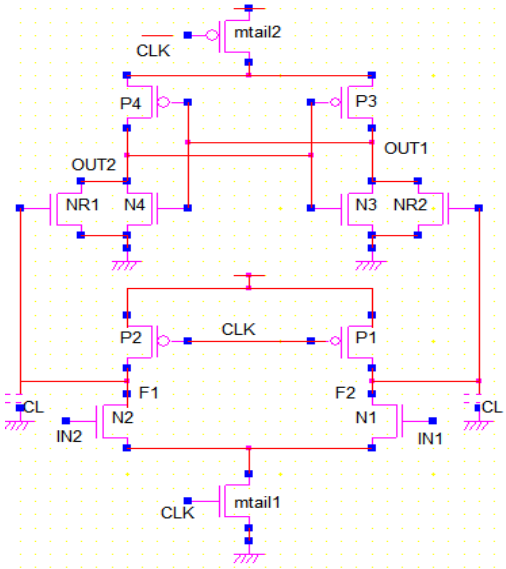


**Fig. 3 Schematic Diagram of Double-Tail Comparator**

The double tail comparator allows both a large current path in the latching stage for fast latching independent of the input common-mode voltage (Vcm), and a small current path in the input stage for low offset. The operation of this comparator is as follows.

### 3.1 Operation

During reset phase, CLK = 0, thus the two tail transistors $m_{tail1}$, and $m_{tail2}$ are off, and the transistors $p_1$ and $p_2$ are on so that the two nodes $f_n$ and $f_p$ will be pre charged to VDD, which in turn causes transistors $NR_1$ and $NR_2$ to discharge the output nodes to ground. During decision-making phase CLK=$V_{DD}$, the transistors $m_{tail1}$ and $m_{tail2}$ will be turned on, and both the PMOS transistors $p_1$ and $p_2$ will be off and voltages at nodes fn and fp start to drop with different rates. The discharging rate at which the voltage drops will be defined by $I_{mtail1}/C_{fn(p)}$ and therefore an input-dependent differential voltage $\Delta V_{fn(p)}$ will build up. The intermediate stage transistors $NR_1$ and $NR_2$ passes this differential voltage $V_{fn(p)}$ to the latch. The intermediate transistors also provide a good shielding between input and output which results in the reduction of kick-back noise.

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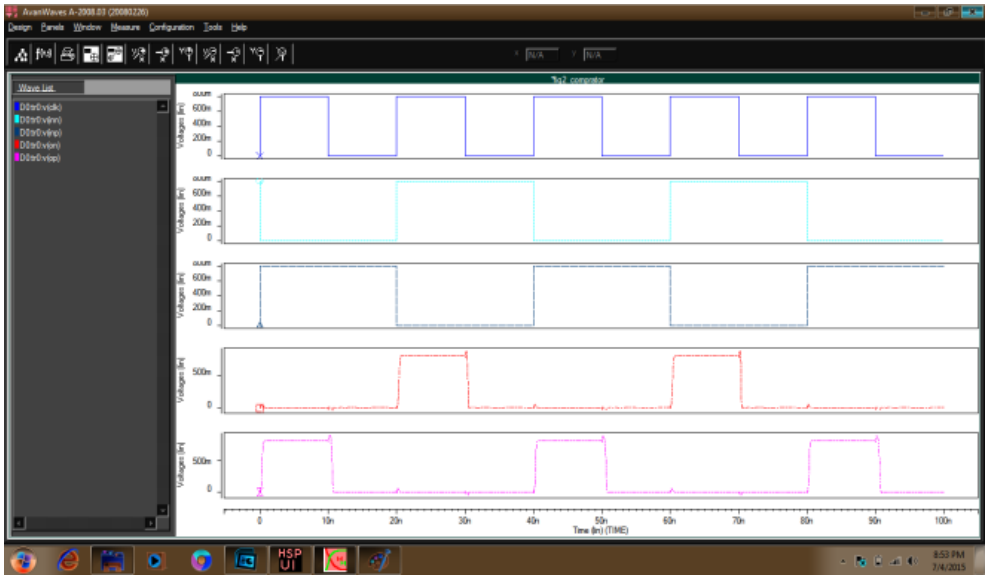

**Fig. 4 Simulation Result of Double Tail Comparator**

The total delay of this comparator can be derived as,

$$t_{delay} = t_0 + t_{latch} = 2\frac{V_{Thn}C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff}}\ln\left(\frac{V_{DD}/2}{\Delta V_0}\right)$$

$$= 2\frac{V_{Thn}C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff}}\ln\left(\frac{V_{DD}I_{tail2}{}^2C_{L,fn(p)}}{8V_{Thn}{}^2C_{Lout}g_{mR1,2}g_{m1,2}\Delta V_{in}}\right) \quad (2)$$

From the equations derived for the delay of the double-tail dynamic comparator, some important notes can be concluded.

1) The latch initial differential output voltage (ΔV0) and consequently the latch delay will be affected by the voltage difference at the first stage outputs (ΔVfn/fp) at time $t_0$. Therefore, increasing it would profoundly reduce the delay of the comparator.
2) In this comparator, both intermediate stage transistors will be cut-off finaly, (since fn and fp nodes both discharge to the ground), hence they do not play any role in improving the effective transconductance of the latch. On the other hand, during reset phase, the nodes fn and fp have to be charged from ground to $V_{DD}$, which means power consumption.

The following section describes how the comparator improves the performance of the double-tail comparator from the above points of view.

## IV. DOUBLE-TAIL DYNAMIC COMPARATOR FOR LOW POWER

Fig. 5 demonstrates the schematic diagram of the dynamic double-tail comparator for low power. This comparator is designed based on the double-tail structure due to the better performance of double-tail architecture in low-voltage application. Two control transistors (PC1 and PC2) have been added to the first stage in parallel to P1/P2 transistors but in a cross-coupled manner in order to increase the latch regeneration speed.

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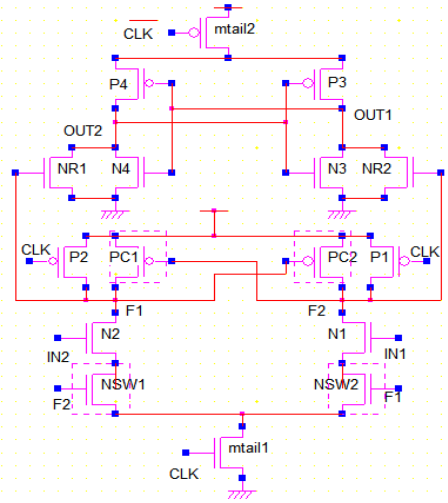


**Fig. 5 Schematic of Double Tail Comparator for Low Power**

### 4.1 Operation

The operation of this comparator is as follows. In the reset phase, CLK = 0, ntail1 and ntail2 are off, P1 and P2 pulls both fn and fp nodes to $V_{DD}$, hence transistor Pc1 and Pc2 are cut off. Intermediate stage transistors, NR1 and NR2, bring both latch outputs to ground. During comparison phase (CLK = $V_{DD}$, Ntail1, and Ntail2 are on), transistors P1 and P2 turn off. Moreover, at the beginning of this phase, the control transistors are still off (since fn and fp are about $V_{DD}$). Thus, according to the input voltages, fn and fp start to drop with different rates. Consider IN1 > IN2, then fn drops faster than fp, since N1 provides more current than N2. When fn falls below the threshold voltage, the corresponding PMOS control transistor (Pc1 in this case) starts to turn on, pulling fp node back to the $V_{DD}$; thus another control transistor (Pc2) remains off, which allows fn to be discharged completely. In other words, in the previous double-tail dynamic comparator, ΔVfn/fp is just a function of input transistor transconductance and input voltage difference, in this structure as soon as the comparator detects that the node fn discharges faster, a PMOS transistor (Pc1) turns on, pulling the other node fp back to the $V_{DD}$.

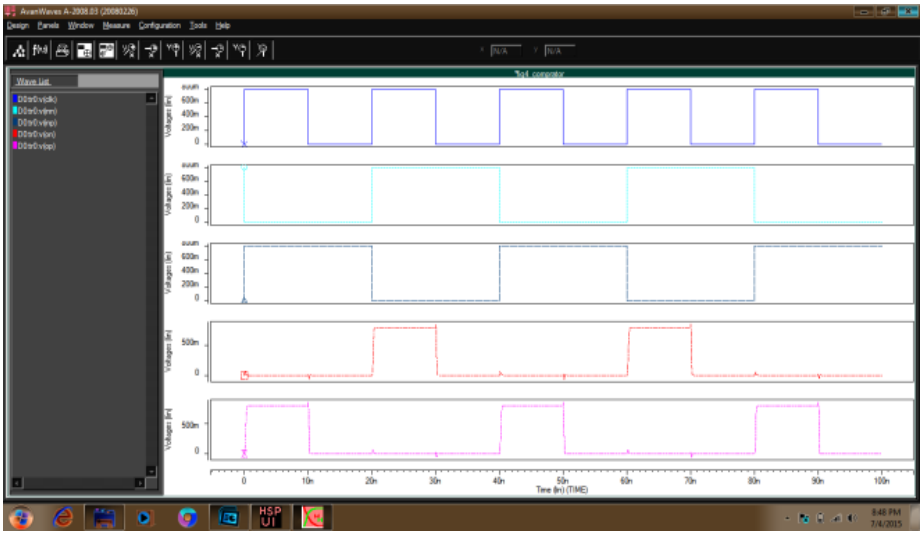

**Fig. 6 Simulation Result of Double tail Comparator for Low Power**

Therefore as this continuous to happen, the difference between fn and fp (ΔVfn/fp) increases in an exponential manner, which leads to the reduction of latch regeneration time. One of the points which should be considered is

that in this circuit, a current from $V_{DD}$ is drawn to the ground via input and tail transistor (e.g., Pc1, N2, and Ntail1), when one of the control transistors (e.g., Pc1) turns on, resulting in static power consumption. To overcome this, two NMOS switches are used below the input transistors [Nsw1 and Nsw2, as shown in Fig. 5]. When the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will increase their voltage difference. Suppose that fp is pulling up to the $V_{DD}$ and fn should be discharged completely, hence in order to prevent any current drawn from $V_{DD}$ the switch in the charging path of fp will be opened but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches imitates the operation of the latch. This will be more discussed in the following section.

Finally, by including both effects, the total delay of the proposed comparator is achieved from

$$t_{delay} = t_0 + t_{latch}$$

$$t_{dealy} = 2\frac{V_{Thn}C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff}+g_{mR1,2}} \ln\left(\frac{V_{DD}/2}{4V_{Thn}|V_{Thp}|\frac{g_{mR1,2}g_{m1,2}\Delta V_{in}}{I_{tail2}\,I_{tail1}}exp\left(\frac{C_{m,eff1}t_0}{C_{L,fn(p)}}\right)}\right) \quad (3)$$

By comparing the expressions derived for the delay of the three mentioned structures, we can say that this comparator takes advantage of an inner positive feedback in double-tail operation and it also strengthens the whole latch regeneration. This speed improvement can be observed more in lower supply voltages. Because for larger values of $V_{Th}/V_{DD}$, the transconductance of the transistors decreases, then the existence of an inner positive feedback in the architecture of the first stage will lead to the improved performance of the comparator circuit. Simulation results confirm this matter.

## V. SUB-THRESHOLD CONDUCTION

As technology scales down, the size of transistors has been shrinking. The number of transistors on chip has thus increased to improve the performance of circuits. In order to maintain the characteristics of an MOS device, the supply voltage, being one of the critical parameters, has also been reduced accordingly. Therefore the threshold voltage is also scaled down at the same rate as the supply voltage in order to maintain the transistor switching speed. As a result, leakage currents increase drastically with each technology generation. As the leakage current increases faster, it will become more and more proportional to the total power dissipation.

$$P_{LEAK} = I_{LEAK} * V_{DD}$$

To reduce total leakage in nanoscale circuits, some new techniques have to be developed to reduce the subthreshold leakage especially for chips that are used in portable systems which are power constrained. The leakage current consists of reverse bias diode currents and Sub-threshold current. The reverse bias current is due to the stored charge between the drain and bulk of active transistors while the Sub-threshold current is due to the carrier diffusion between the source and drain of the off transistors. Hence, in this paper conventional CMOS inverter based approach is used to reduce the Sub-threshold leakage power.

## VI. DOUBLE-TAIL COMPARATOR WITH REDUCED LEAKAGE POWER

The amplifier circuit is modified according to the inverter logic. The inverter logic which reduces the leakage is shown in fig 7. Here, two inverters are used. The inputs are applied to two inverters and the outputs are connected

to a active load. The circuit will be used in our double tail comparator structure. The differential amplifier will be modified with this inverter logic. The output will be applied to the latch for regeneration.

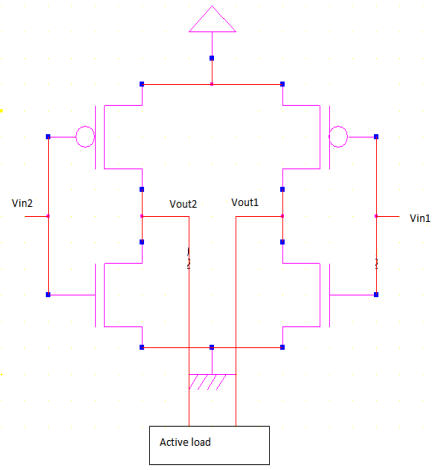


**Fig.7 Inverter Based Amplifier Design**

The differential amplifier circuit is modified with this inverter logic. Now the total circuit of Double Tail Comparator becomes as

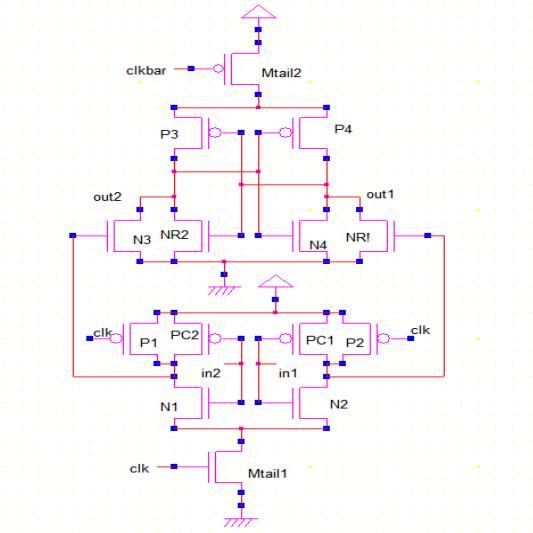


**Fig. 8 Schematic of Double Tail Comparator with Reduced Leakage Power**

### 6.1. Operation

During reset phase, when CLK=0, $M_{tail1}$ and $M_{tail2}$ are off and $P_1$ and $P_2$ are on so that the two transistors $NR_1$ and $NR_2$ will be on and pulls the two output nodes out1 and out2 to ground. During decision making phase, when CLK=$V_{DD}$, the two tail transistors $M_{tail1}$ and $M_{tail2}$ are on and P1 and P2 are off which turns the two transistors NR1 and NR2 off. Consider the case where IN1>IN2, then the transistors $N_2$ will turn on faster so the output of that inverter falls down which turns the intermediate transistor $NR_1$ off. Hence, out1 pulls up to $V_{DD}$. When out1 goes to $V_{DD}$, the transistor p3 will be off which remains out2 at ground. By using this approaches the Sub-threshold leakage and hence the total power will be reduced. The simulation results prove the reduction. Here in the differential amplifier inverters are used which are series transistors. Hence, the transconductance of the total circuit

increases which reduces the total delay of the circuit. Hence, by using this CMOS inverter approach the total power and delay can be reduced. The simulation results show the reduction in both power and delay.

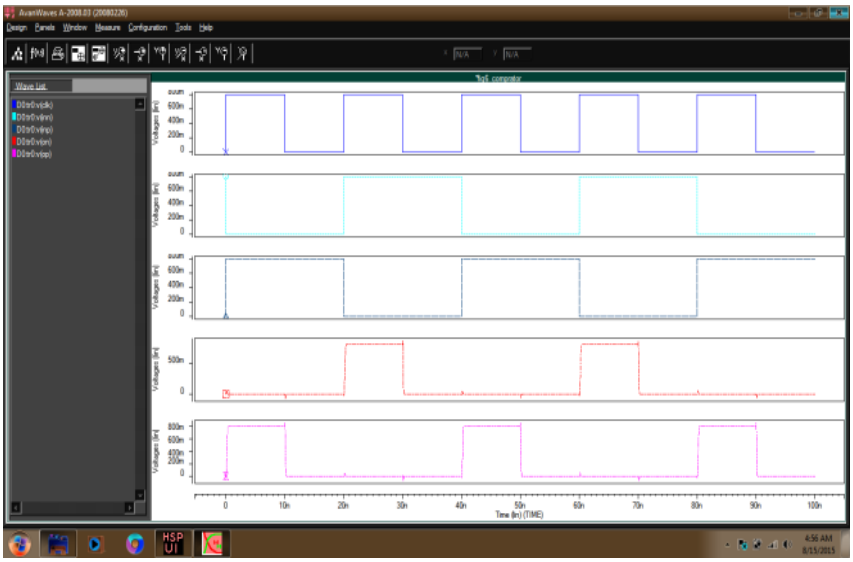

**Fig. 9 Simulation Results of Double Tail Comparator with Reduced Leakage**

Fig. 10 shows the layout of proposed structure

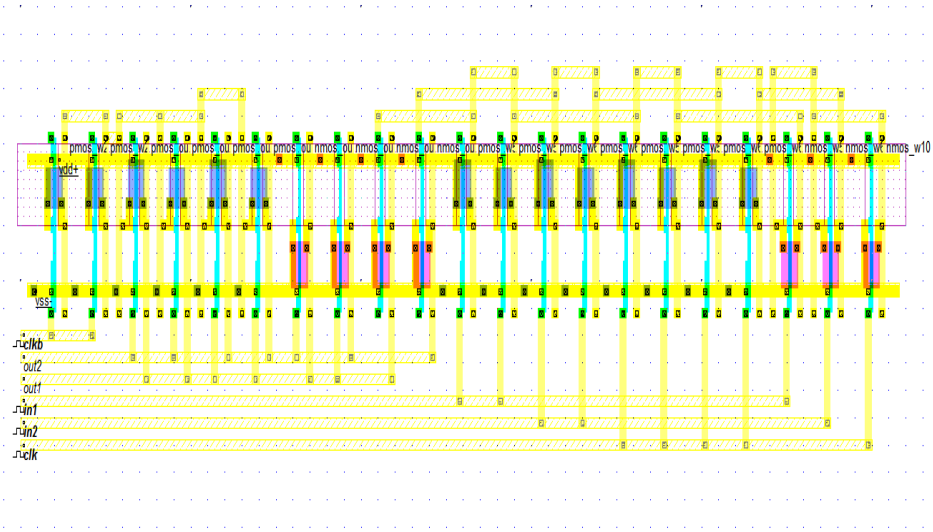


**Fig. 10 Layout of Proposed Structure**

**Table 1: Comparison of Results**

| comparator structure | Single-Tail Comparator | Double-Tail Comparator | Double-Tail comparator with lov power | Double tail comparator with reduced leakage |
|---|---|---|---|---|
| Technology | 120nm | 120nm | 120nm | 120nm |
| Supply voltage | 0.8V | 0.8V | 0.8V | 0.8V |
| Delay | 534.47ps | 319.66ps | 224ps | 196.4ps |
| Power | 560 | 855 | 444 | 391 |
| Layout Area | 156.42μm$^2$ | 227.84 μm$^2$ | 330.88 μm$^2$ | 294.22 μm$^2$ |

Table 1 shows the simulated results of all the comparators mentioned.

## VII. CONCLUSION

The delay of clocked comparators was analyzed and equations were derived. Dynamic latched comparator was designed that works with high speed and low power when compared to previous comparators. The simulation results showed that the proposed circuit can operate at higher speed with low power dissipation. Compared to the conventional structure, the proposed method occupies less chip area. A CMOS inverter based amplifier design was implemented to reduce the sub threshold leakage. The simulation results confirmed the analysis and showed that in the proposed dual tail dynamic comparator both power consumption and delay time are significantly reduced even in small supply voltage. The Power and delay of each circuit were measured and compared. Now we can conclude that the proposed comparator is delay efficient, power efficient and area effective also.

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