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AN EFFICIENT VLSI ARCHITECTURE FOR 64-BIT VEDIC MULTIPLIER

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ABSTRACT

*Multipliers are very significant part of any processor or computing device and DSP processor. Reversible logic circuits have many applications in quantum computing, nanotechnology and low power CMOS technology, optical information processing. A system's performance is generally determined by the performance of the multiplier. Here the multipliers are implemented using reversible gates. Therefore better multiplier architecture are assured to increase the capability of the device.in many processors and DSP processors systems need to develop low power multipliers to reduce the power dissipation. And also multiplier architectures are bound to increase the efficiency of the system. Vedic multiplier is one such solution, its simple architecture with increased speed forms an unparalleled combination for serving any complex multiplications computations. Here the vedic multiplier is known as "urdhya tiryakbhayam" meaning vertical and crosswise, implemented using reversible logic vedic multiplier with 4,8,16,32,64 bit sizes, it can multiply up to N*N multiplications.*

***Keywords*: Vedic Multiplier, Reversible Logic Gates, Urdhya Tiryakbhayam, Ripple Carry Adder.**

I.INTRODUCTION

Multiplication is the most basic and frequently used operations in CPU. Scaling of one number with another number is the operation of Multiplication. Multiplication also supports for complex operations such as convolution, Discrete Fourier Transform, Fast Fourier Transform etc. The advancement in technology there is a need of increasing faster clock frequency to have faster arithmetic unit. The fastness of the arithmetic unit depends mainly on the performance of multipliers and adders. To achieve efficient performance high speed multipliers of different types are available. The multipliers mainly use the concept of vedic mathematics on reversible logic gates.

1.1 Vedic Mathematics

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It gives explanation of several mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus.[7] His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884- 1960) comprised all this work together and gave its mathematical explanation while discussing

it for various applications. Swamiji constructed 16 sutras (formulae) and 16 Up a sutras (sub formulae) after extensive research in Atharva Veda. Obviously these formulae are not to be found in present text of Atharva Veda because these formulae were constructed by Swamiji himself. Vedic mathematics is not only a mathematical wonder but also it is logical. That's why it has such a degree of eminence which cannot be disapproved. Due these phenomenal characteristics, Vedic maths has already crossed the boundaries of India and has become an interesting topic of research abroad. Vedic maths deals with several basic as well as complex mathematical operations. Especially, methods of basic arithmetic are extremely simple and powerful. The word "Vedic" is derived from the word "Veda" which means the store-house of all knowledge. Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc [11]. These Sutras along with their brief meanings are enlisted below alphabetically.

a. (Anurupye) Shunyamanyat – If one is in ratio, the other is zero.
b. Chalana-Kalanabyham – Differences and Similarities.
c. Ekadhikina Purvena – By one more than the previous One.
d. Ekanyunena Purvena – By one less than the previous one.
e. Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.
f. Gunitasamuchyah – The product of the sum is equal to the sum of the product.
g. Nikhilam Navatashcaramam Dashatah – All from 9 and last from 10.
h. Paraavartya Yojayet – Transpose and adjust.
i. Puranapuranabyham – By the completion or noncompletion.
j. Sankalana- vyavakalanabhyam – By addition and by subtraction.
k. Shesanyankena Charamena – The remainders by the last digit.
l. Shunyam Saamyasamuccaye – When the sum is the same that sum is zero.
m. Sopaantyadvayamantyam – The ultimate and twice the penultimate.
n. Urdhva-tiryagbhyam – Vertically and crosswise.
o. Vyashtisamanstih – Part and Whole.
p. Yaavadunam – Whatever the extent of its deficiency.

These methods and ideas can be directly applied to trigonometry, plain and spherical geometry, conics, calculus (both differential and integral), and applied mathematics of various kinds. As mentioned earlier, all these Sutras were reconstructed from ancient Vedic texts early in the last century. Many Sub-sutras were also discovered at the same time, which are not discussed here. The beauty of Vedic mathematics lies in the fact that it reduces the otherwise cumbersome-looking calculations in conventional mathematics to a very simple one. [5]This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing. The multiplier architecture can be generally classified into three categories. First is the serial multiplier which emphasizes on hardware and minimum amount of chip area. Second is parallel multiplier (array and tree) which carries out high speed mathematical

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operations. But the drawback is the relatively larger chip area consumption. Third is serial- parallel multiplier which serves as a good trade-off between the times consuming serial multiplier and the area consuming parallel multipliers.

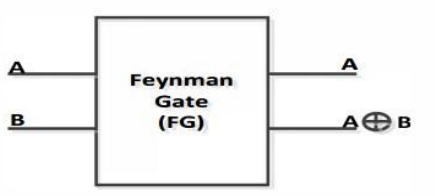
1.2. Reversible Logic

Reversible logic is a promising computing design paradigm which presents a method for constructing computers that produce no heat dissipation. Reversible computing emerged as a result of the application of quantum mechanics principles towards the development of a universal computing machine. Specifically, the fundamentals of reversible computing are based on the relationship between entropy, heat transfer between molecules in a system, the probability of a quantum particle occupying a particular state at any given time, and the quantum electrodynamics between electrons when they are in dose proximity. The basic principle of reversible computing is that a bi-jective device with an identical number of input and output lines will produce a computing environment where the electrodynamics of the system allow for prediction of all future states based on known past states, and the system reaches every possible state, resulting in no heat dissipation A reversible logic gate is an N-input N-output logic device that provides one to one mapping between the input and the output. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs. Garbage outputs are those which do not contribute to the reversible logic realization of the design. Quantum cast refers to the cost of the circuit in terms of the cost of a primitive gate. Gate count is the number of reversible gates used to realize the function. Gate level refers to the number of levels which are required to realize the given logic functions. The following are the important design constraints for reversible logic circuits.

I. Reversible logic gates do not allow fan-outs.
2. Reversible logic circuits should have minimum quantum cost.
3. The design can be optimized so as to produce minimum number of garbage outputs.
4. The reversible logic circuits must use minimum number of constant inputs.
5. The reversible logic circuits must use a minimum logic depth or gate levels. The basic reversible logic gates encountered during the design are listed below:

1.2.1. Feynman Gate

It is a 2x2 gate and its logic circuit is as shown in the figure. It is also known as Controlled Not (CNOT) Gate. It has quantum cost one and is generally used for Fan Out purposes.



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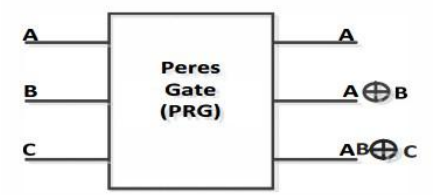
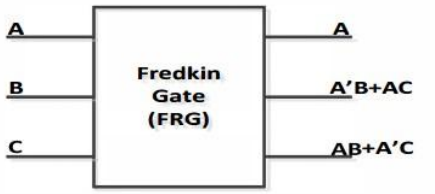
1.2.2. Peres Gate

It is a 3x3 gate and its logic circuit is as shown in the figure. It has quantum cost four. It is used to realize various Boolean functions such as AND, XOR.



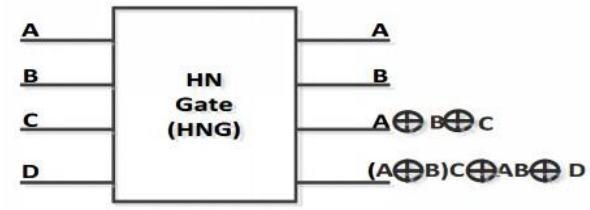
1.2.3. Fredkin Gate

It is a 3x3 gate and its logic circuit is as shown in the figure. It has quantum cost five. It can be used to implement a Multiplexer.



1.2.4. HNG Gate

It is a 4x4 gate and its logic circuit is as shown in the figure. It has quantum cost six. It is used for designing ripple carry adders. It can produce both sum and carry in a single gate thus minimizing the garbage and gate counts.



1.3. Vedic Multiplication Using Urdhva- Tiryakbhayam Algorithm

Operation of Vedic multiplier depends upon the Vedic sutras which were reconstructed by Shree Bharati Krishna. Urdhva- tiryakbhayam is the multiplication sutra (algorithm) in Vedic mathematics.Urdhva means vertical. Triyakbhyam means Crosswise. The multiplier is based on an algorithm Urdhva- tiryakbhyam (Vertical and Crosswise) of Vedic Mathematics. Urdhva-tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It accurately means vertically and crosswise. It is based on a novel concept through which the generation of all partial products can be done with the simultaneous addition of these partial products. The algorithm can be generalized for n × n bit number. [1][3]

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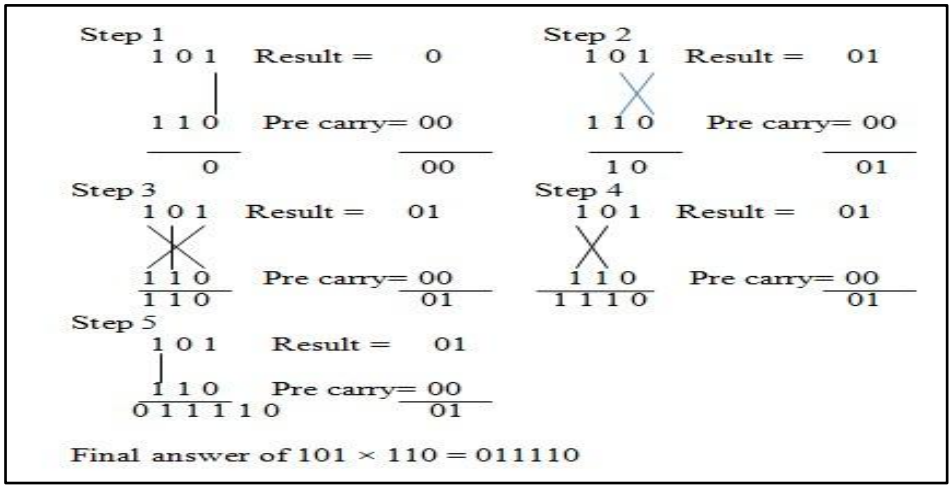
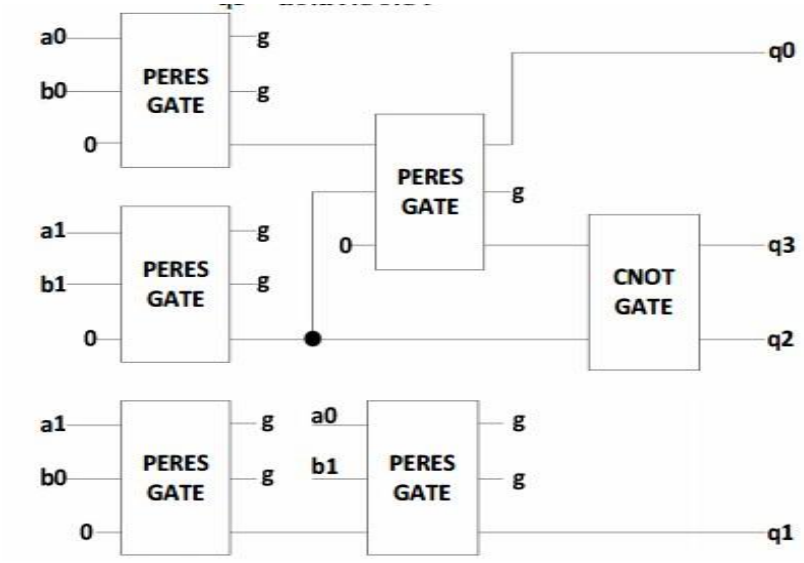
Unlike other multipliers with the increase in the number of bits of multiplicand and/or multiplier the time delay in calculation of the product does not increase proportionally. Because of this fact the time of calculation is independent of clock frequency of the processor. Hence one can limit the clock frequency to a lower value. Below figure shows Urdhva Tiryagbhyam algorithm for binary multiplication



1.4. Reversible Implementation



The Reversible 4X4 Urdhva Tiryakbhayam Multiplier design from the 2X2 multiplier. The block diagram of the 4X4 Vedic Multiplier is presented in the figure. It consists of four 2X2 multipliers each of which procedures four bits as inputs; two bits from the multiplicand and two bits from the multiplier. The lower two bits of the output of the first 2X2 multiplier are entrapped as the lowest two bits of the final result of multiplication. And second multiplier output, third multiplier output given as input to the four bit ripple carry adder then get output. Adder output and first multiplier output add three zeros are given as input to five input bits ripple carry adder then get output. Adder output and fourth multiplication given as input four bit ripple carry adder. These six bits from the upper bits of the final result. The ripple carry adder is consummated (realized) using the HNG Gate.

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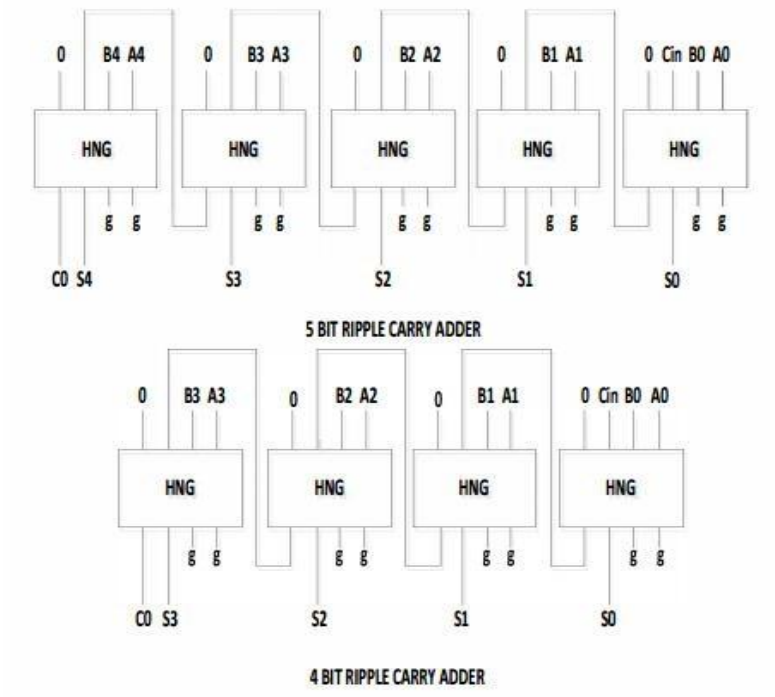
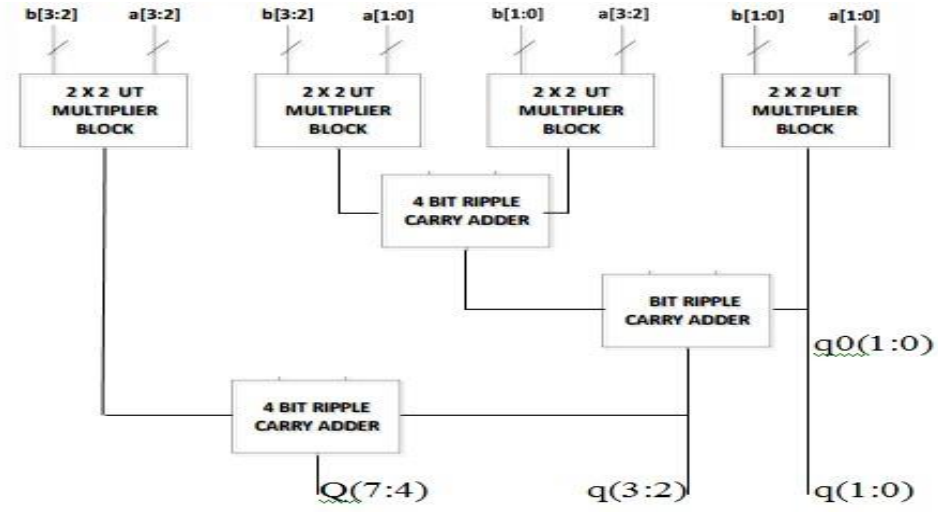
The number of bits that need to be ripple carried verdicts the number of HNG gates to be used. Thus a 4 bit ripple carry adder needs 4 HNG gates and the 5 bit adder requires 5 HNG gates. This design also does not take into consideration the fan out gates. For this design the quantum cost is computed to be 162, the total number of gates used will be 37, the number of garbage outputs will be 62 and the number of constant inputs will be 29.



1.4.1. 4X4 Multiplier



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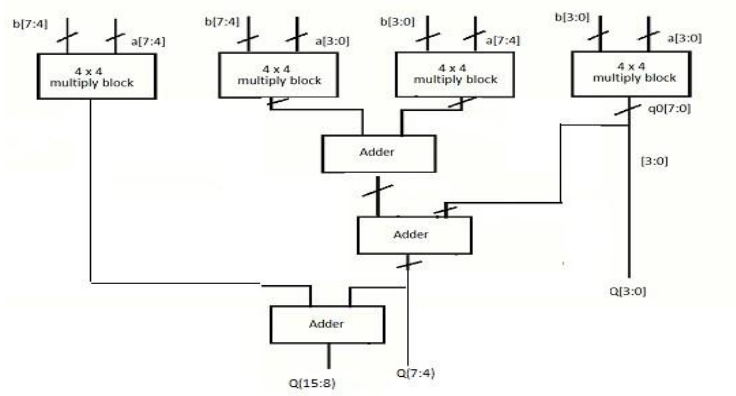
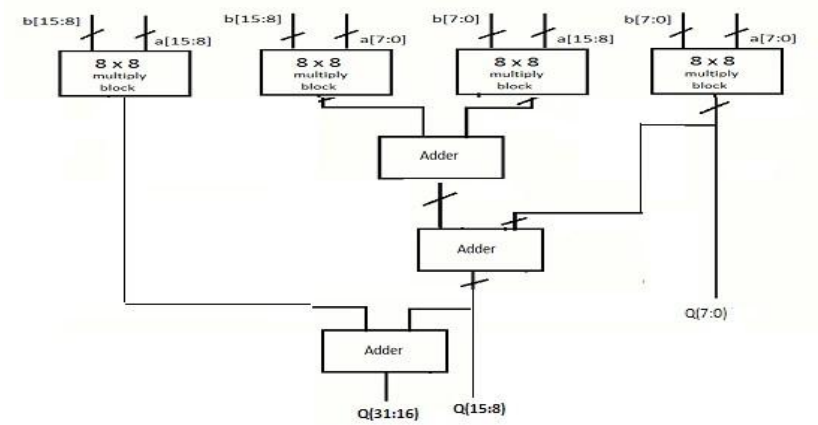
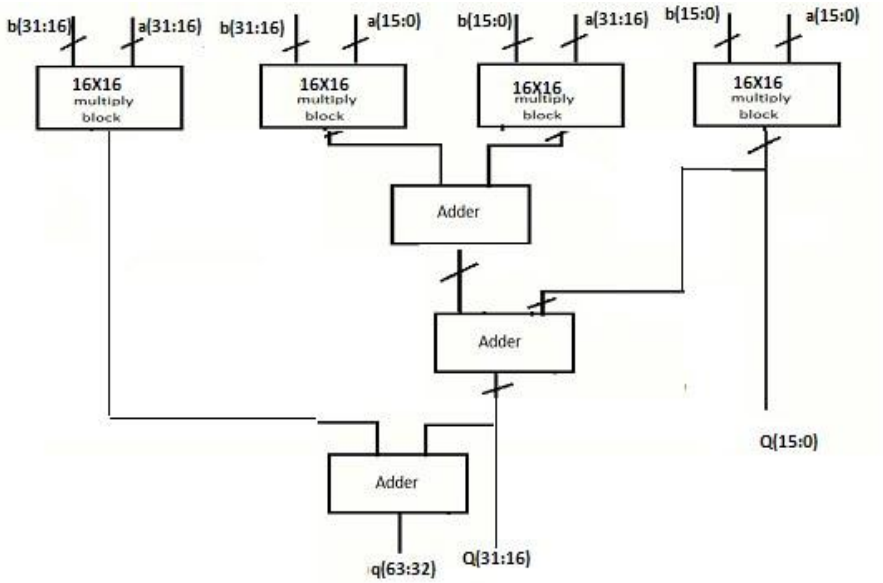
8X8 Multiplier



1.4.2. 16X16 Multiplier



1.4.3 32X32 Multiplier



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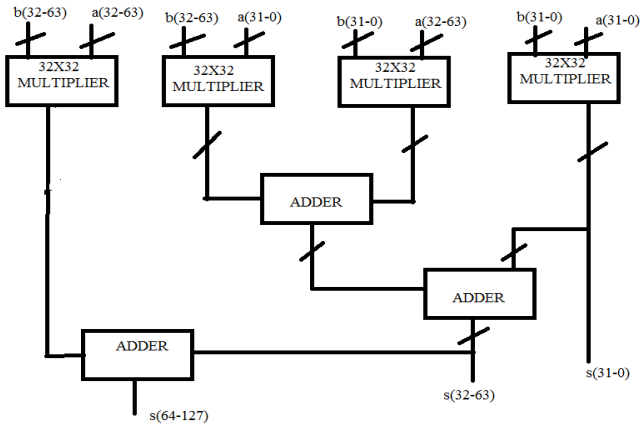
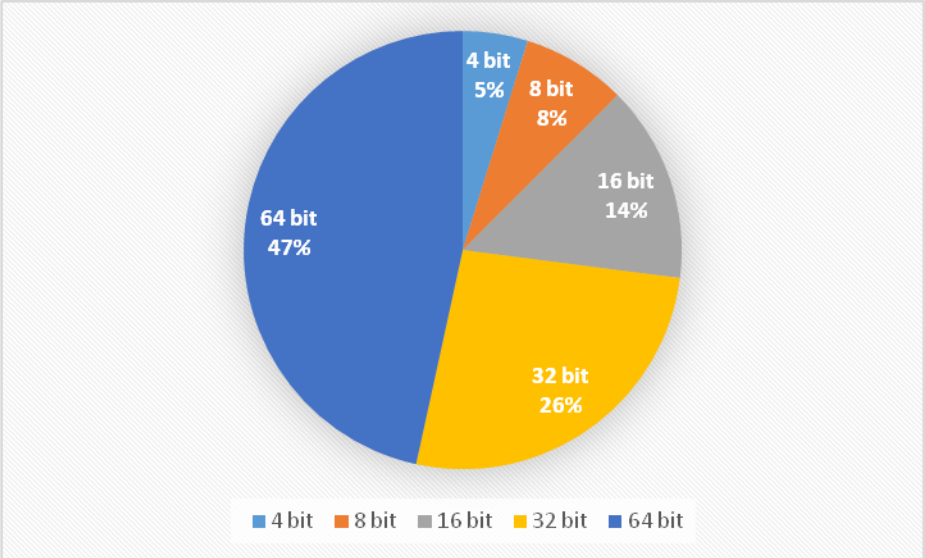
1.4.4. 64x64 Multiplier



1.4.5. Power Delay Product



BIT COUNT	DELAY
4 bit	3.128 ns
8 bit	5.021 ns
16 bit	9.466 ns
32 bit	17.184 ns
64 bit	30.343 ns

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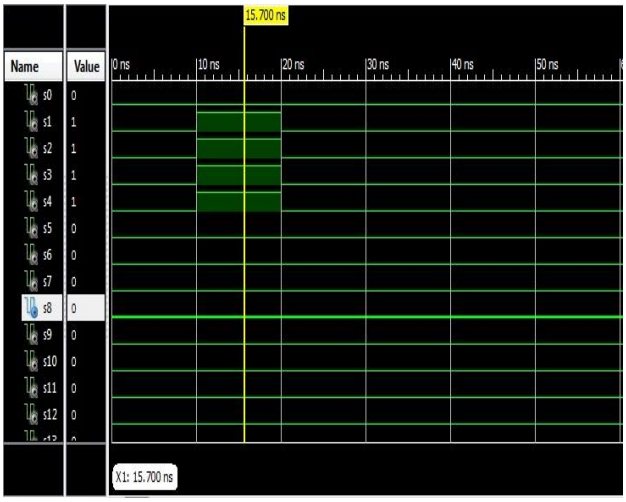
1.4.6. Simulated Output: (64 BIT)



The above figure shows the simulated output of 64x64 UT multiplier using Xilinx.

II.CONCLUSION

The Urdhva Tiryakbhayam Vedic Multiplier realized using reversible logic gates. Firstly a basic 2x2 UT multiplier is designed. After this, the 2x2 UT multiplier block is cascaded to obtain 4x4 multiplier. The 4x4 UT multiplier block is cascaded to obtain 8x8 multiplier. The 8x8 UT multiplier block is cascaded to obtain 16x16 multiplier. The 16x16 UT multiplier block is cascaded to obtain 32x32 multiplier. The 32X32 UT multiplier block is cascaded to obtain 64x64 multiplier.The ripple carry adders which were required for adding the partial products were constructed using HNG gates.

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