International Journal of Electrical and Electronics Engineers
Vol. No. 9, Issue No. 01, January-June 2017
ISSN (O) 2321-2055
ISSN (P) 2321-2045

A HIGH SPEED & LOW POWER 16T 1-BIT FULL ADDER CIRCUIT DESIGN BY USING MTCMOS TECHNIQUE IN 45nm TECHNOLOGY

Jasbir kaur[1], Neeraj Singla[2]

[1]Assistant Professor , [2]PG Scholar

Electronics and Communication Department, PEC University of Technology, Chandigarh

ABSTRACT

A 16T full adder circuit has been designed and analysed in this paper. It contains Transmission as well as inverter in its circuit.16T circuit has low power and high performance than the conventional one. The designed circuit consist of multi-threshold complementary metal oxide (MTCMOS) technique to increase the performance and to reduce the power consumption of the conventional circuit. The circuits designed by MTCMOS has high speed and low power consumption by using transistors having low and high threshold voltages. Leakage power of 16T adder is reduced by 49.9% designing the circuit through MTCMOS as compared to standard adder. Implementation and analysis is based on 45nm in cadence virtuoso tool.

Keywords-16T 1 bit full adder, Multi-threshold CMOS, High speed, low power

I. INTRODUCTION

At Fairchild semi-conductor the first Integrated circuit was invented in 1959. The assembly of full electronic circuits on a single chip significantly increase performance and reliability as compared the discrete components. Gordon Moore stated that various advancements in integrated circuit (IC) technology in 1965 and the market dynamics was the key reason for the growth of semiconductor technology. Since 1970's integration density (no. of components) increased by every two or three years, caused increase in speed and technology. Reduction in size (technology scaling) in the key factors on integration density of the circuit.

For portable devices a low power design is essential for longer run. As technology has scaled down in nm regime, power dissipation has becomes the major issue of discussion. Scaling down of technology leads to lower the power supply and threshold voltages caused significant growth in leakage power. This forced scientists to adapt new methodology to meet new power constraints.

The current flowing through a transistor, even in off condition causes sub threshold leakage which is a major component of leakage power. The effect of the sub-threshold leakage increases as the size of transistor is scaled down.

There are lots of techniques that have been proposed to reduce leakage power. This problem not only caused overheating, reduces battery life, decrease functionality, minimizes performance as well as degrades chip life. Reduction in power dissipation is necessary and important both for increasing level of circuit density, reliability

International Journal of Electrical and Electronics Engineers
Vol. No. 9, Issue No. 01, January-June 2017
ISSN (O) 2321-2055
ISSN (P) 2321-2045

and cost, feasibility. Here in this paper the proposed technique for high speed and low power for designing 16T full adder is MTCMOS in 45nm regime. MTCMOS technique has been evolved to construct as very reliable techniques high speed with smaller power consumption as compared to standard 16T full adder. MTCMOS has low and threshold voltages CMOS used to enhance performance and provide low design methodologies. MTCMOS is very effective technique as compared to other techniques

This paper has organized as follows section2 gives a brief description of analysis of conventional 16T full adder and section3 presents 16T adder with proposed MTCMOS Technique. Section4 introduces the concept of leakage power of 16T full adder circuit and details of leakage current Section5 shows the schematic and simulation results of 16T adder using MTCMOS.

II. IMPLEMENTATION OF 16T FULL ADDER USING CMOS TECHNOLOGY.

The most fundamental operation in any circuit is addition and this operation is performed by an adder. An adder is a digital logic circuit in electronics that implements addition of numbers. In many computers and other types of processors, adders are used to calculate addresses, similar operations and table indices in the ALU and also in other parts of the processors. These can be built for many numerical representations like excess-3 or binary coded decimal. To increase speed and minimize power consumption features of adder should be well establishedIn digital circuit theory, combinational logic is a circuit which implements Boolean expression. This expression presents outputs depends upon the present input only. Whereas in sequential circuit the output depends upon the present as well as past input. Hence, sequential circuit has memory and combinational circuit has not.

To do Boolean algebra on stored data and input signal Combinational circuit is used. But in actual computation is combination of both sequential and combination circuit. All the adders (half adder, half sub-tractors, full adders, full sub -tractors), multi-plexers, DE multiplexers, decoders and encoders are combinational circuit whereas flip-flip, counters, registers is known as sequential circuit.

A. Implementation Of 16transmission Full Adder Using Logic Gates

The 16t full adder is built of two types of logic gates inverter and transmission gate. 16T is three input adder (A, B, Cout) and as the name says itself, it uses 16 transistors. It has two outputs sum and carry. The circuit diagram of 16T depicted in fig1. shown below incorporates transmission gates which provides low resistance path and passes strong 0 and strong 1 at the output, inverters and pass transistors. It is highly recommended to use 16T full adder when it comes about performance in terms of leakage power and leakage current. The four basic operation of addition is:

0+0=0

0+1=1

1+0=1

1+1=0

The expression of 16T full adder can be derived from the circuit diagram. Sum of products of expressions are:

International Journal of Electrical and Electronics Engineers
Vol. No. 9, Issue No. 01, January-June 2017
ISSN (O) 2321-2055
ISSN (P) 2321-2045

Sum=(A xnor B)C +C'(A xor B)

Carry=(A xor B)C+(A xnor B)A

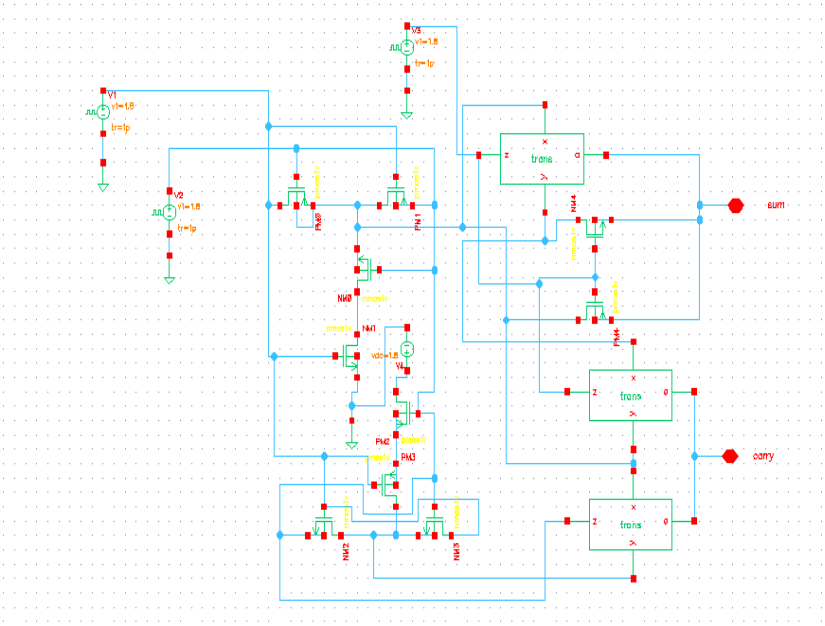

FIG1. 16T FULL ADDER CIRCUIT

TABLE 1. TRUTH TABLE OF 16T FULL ADDER

A	B	CarryIn	CarryOut	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

B. Logic Gates Description for Implementation 16t Full Adder

1) Transmission gate:

A transmission gate also known as analog switch which either passes an input signal (ON state) or blocks input (OFF state).TG is a combination of pull-up (PMOS) and Pull-down Transistor. The connections of these transistors are such that both works in complementary manner i.e. both are either off or on.

The schematic of TG is shown in fig 2:

International Journal of Electrical and Electronics Engineers
Vol. No. 9, Issue No. 01, January-June 2017
ISSN (O) 2321-2055
ISSN (P) 2321-2045

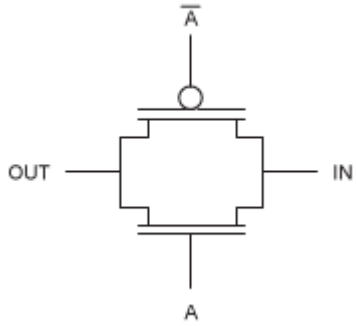

Fig 2. Transmission Gate

When logic 1 is applied at node A, the complementary Logic 0 is applied at its active low pin, causes conduction of both the transistors. And passes high signal from IN to OUT. When Logic 0 is applied at node A, its complementary value Logic 1 is applied to other terminal (active low pin), turns both the transistor OFF and OUT is zero. Applying high impedance condition on IN and OUT is its third state known as High impedance state. Thus TG has three states (high, low, High-Z).

Table 2. Truth Table of Transmission Gate

A	IN	OUT
H	H	H
H	L	L
L	X (don't care)	Z(high impedance)

2. Inverter

Inverter is used in most of the circuits as fundamental part in any Boolean logic circuit design to perform various logic operations such as Nand, Nor which are implemented according to its structure. Hence it's very necessary to design an efficient inverter cell in terms of performance and speed. In spite of this it's fan in and fan out ratio should also high i.e. driving capability is also very important. The schematic of inverter is shown in fig 3.

International Journal of Electrical and Electronics Engineers
Vol. No. 9, Issue No. 01, January-June 2017
ISSN (O) 2321-2055
ISSN (P) 2321-2045

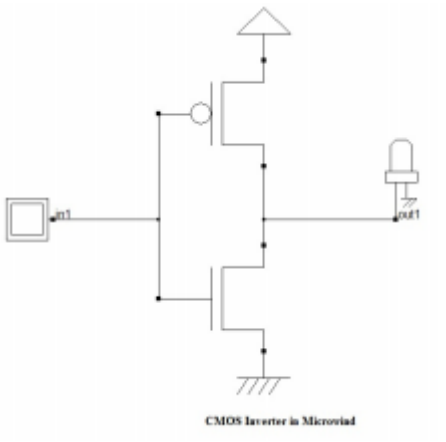

Fig 3. Inverter cell

In CMOS inverter cell both NMOS and PMOS are used simultaneously to provide inverting operation, both the MOS are complementary to each other. When input is at logic '1' at NMOS (pull down network) , led directly connects to gnd ,when logic "1" input is given to PMOS (pull up network) then cell act as an active switch directly connects to V_{dd} and LED glow

Table 3. Truth Table of Inverter

INPUT	OUTPUT	LED
0 "when switch is off"	1	GLOW
1 "when switch is on"	0	NOT GLOW

III. IMPLEMENTATION OF 16T FULL ADDER USING MTCMOS TECHNIQUE

According to Moore's law, no. of transistors increases by every two year so there is a need to reduce the size of transistor (nanometer regime) as the size reduces power supply and threshold voltage should also be reduced. By lowering the value of threshold there is an exponential increase in leakage power. Due to this power dissipation there is a great effect on battery life of portable devices also leads to overheating, degradation in performance and functionality .In nanometre regime 40% power is dissipated only due to leakage currents. In the modern high performance integrated circuits, more than 40% of the active mode power is dissipated due to the leakage current. With the increased no. of transistor many leakage current comes under picture like sub-threshold conduction current, gate direct tunnelling current, punch-through current. Many techniques have been proposed to reduce these leakages. The most effective technique is MTCMOS.

MTCMOS technique is proposed to satisfy the lower threshold voltage requirement as well as to increase the speed of the circuit. In other words to get high performance and high speed circuit . Hence it has two main advantages. MTCMOS works on two types of principles: One is using NMOS and PMOS of logic circuit with low threshold voltage another is it is used to reduce the leakage power in standby mode which makes the circuit efficient for portable devices to work it for long run

In MTCMOS technique, circuit is virtually connected to power supply and ground by using high threshold voltage transistors i.e circuit is connected to high threshold (Vth) transistor and this High threshold voltage transistor connects directly to Vdd and Gnd. The block diagram of MTCMOS circuit is shown fig4. These High

International Journal of Electrical and Electronics Engineers
Vol. No. 9, Issue No. 01, January-June 2017
ISSN (O) 2321-2055
ISSN (P) 2321-2045

Vth is powered by sleep signal. The main logic circuit is made of Low Vth transistors. When the circuit is on active mode ,the circuit with low Vth transistors is on through this high Vth transistors, and when the circuit is in inactive mode both high Vth are OFF making the circuit disconnected to Vdd and Gnd. This causes reduction in leakage current when circuit is in standby mode. Other main feature is as the threshold voltage is reduced, the circuit operates faster, that means smaller the threshold voltage, smaller is the delay. So, from the view point of performance, it is essential to have smaller threshold voltage. Smaller threshold voltage in a circuit leads to faster operation and higher performance. The disadvantage of MTCMOS is sizing of the transistors.

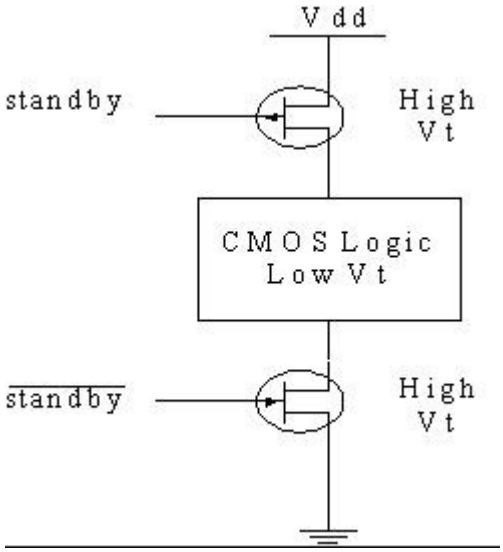

FIG 4. General Mtcmos circuit architecture

The circuit diagram of 16T MTCMOS is shown in Fig 5:

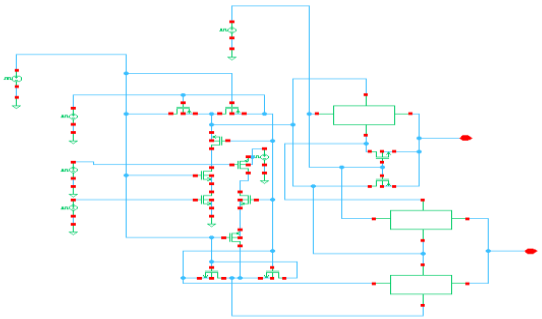

Fig 5: 16T MTCMOS Full adder

IV. CONCEPT OF LEAKAGE POWER

Leakage power is the major issue in all the CMOS design circuit. Leakage power can be reduced by reduction in node voltages. In other words, it can be deducted that leakage power is basically the charge wasted (leads to discharges the circuit) when the device is in off state. It degrades the functionality, performance, battery life. Hence it becomes the major reason to discussed upon for the portable devices..

As the gate oxide thickness reduces, the leakage power increase exponentially. Another type of leakage current is tunnelling leakage which occurs across junction if N-type and P-type is heavily doped. Carries can also leak

International Journal of Electrical and Electronics Engineers
Vol. No. 9, Issue No. 01, January-June 2017
ISSN (O) 2321-2055
ISSN (P) 2321-2045

through gate insulator. This is known sub threshold conduction. The leakage has been classified into three major parts: junction tunnelling current, sub threshold current, and gate tunnelling current. With the increase in leakage power dissipation, there can be the complete circuit failure. Therefore a circuit should be static power efficient, i. e it must dissipate zero power when in idle mode. Earlier the major issue was speed and area but as the technology reaches below sub-micron power leakage per unit area becomes the main concern. In this paper 45nm technology is used to reduce the power dissipation

The expression for leakage power in dynamic and static mode is

$$\text{Static Power } P_s = I_{leakage} * V_{dd}$$

$$\text{Dynamic Power } P_d = C_L * V_{dd}^2 * F_p$$

Where P = Power Dissipation

I =Leakage current

V =power supply

F =Frequency of operation

C = Parasitic capacitances

V. SIMULATION RESULTS

16Tone bit adder is used to perform three bit addition .In this paper the technology used to design the circuit is 45nm by using Cadence Virtuoso. MTCMOS techniques used effectively reduces the power dissipation as well as increase the speed of the circuit as compared to conventional 16T adder circuit. From simulation results it is observed that MTCMOS technique reduces by 49.9% leakage power in standby mode, and hence can be applied to minimize leakage power.

Table Tv Leakage Power of 16t Full Adder

	16T Conventional	16T MTCMOS
Average Power Dissipation(nW)	95.13	47.63
Average Sum Delay(Ps)	69.64	0.27.66
Average Carry Delay (Ps)	98.54	0. 98.54

VI. CONCLUSION

The power dissipation and delay is the main issue in nm technology. In this paper MTCMOS technique is proposed to reduce these two parameters. From the simulation results it has been observed that leakage power reduce highly in 16T MTCMOS as compared to conventional 16T CMOS full adder. Thus MTCMOS techniques is highly effective to increase the circuit's overall performance by using low and high threshold transistors. From the analysis it can be clearly observed that leakage power reduced by 49.9% compared to conventional circuit.

REFERENCES

[1.] V. Kursun and E. G. Friedman, Multi-Voltage CMOS Circuit Design, John Wiley & Sons Ltd., 2006, ISBN # 0-470-01023-1.

[2.] V. Kursun, "Supply and Threshold Voltage Scaling Techniques in CMOS Circuits", Ph.D Thesis, University of Rochester, 2004.

[3.] Nirmal U., Sharma G., Mishra Y., "Low Power Full Adder using MTCMOS Technique" in proceeding of International conference on advances in Information, Communication Technology and VLSI Design, Coimbatore, India, August 20I O.

[4.] Mutoh S et al "I-V, Power Supply High Speed Digital Circuit Technology with Multithreshold-Voltage CMOS" IEEE J. Solid State Circuits, Vo1.30, pp 847-854,August 1995.

[5.] Yu et aI., "Limits of gate oxide scaling in nano-transistors," in Proc. Symp. VLSI Technol., 2000, pp. 90-91

[6.] Abdollahi A., Fallah F. and Pedram M.,2004,Leakage current reduction in CMOS VLSI circuits by input vector control, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*,*Vol*.12,*No*.2,pp.140-154.

[7.] Jeon H., Kim Y.B. and Choi M., 2010, Standby leakage power reduction technique for nanoscale CMOS VLSI systems, *IEEE transactions on instrumentation and measurement*, Vol.59, No.5, pp.1127-1133.

[8.] Jalan A. and Khosla M., December 2011, Analysis of leakage power reduction techniques in digital circuits, *Annual IEEE India Conference*, pp. 1-4.

[9.] Kalyani P., Satishkumar D.P. and Ragini D.K., 2003, Various Low Power Techniques for CMOS Circuits, *International Journal of Engineering Research and Applications*, pp.2248-9622.

[10.] Liu W., 2007, Techniques for leakage power reduction in nanoscale circuits, *A survey on Informatics and Mathematical Modelling*, Technical University of Denmark, DTU

[11.] Park J.C. and Mooney III, V.J., 2006, Sleepy stack leakage reduction., *IEEE Transactions on very large scale integration (VLSI) systems*,Vol.14,No.11,pp.1250-1263.

[12.] Sivakumar, R. and Jothi, D., 2014, Recent Trends in Low Power VLSI Design", International Journal of Computer and Electrical Engineering, pp.509-513.