REVIEW: DESIGN OF HIGH RADIX ADDITION IN DEEP SUBMICRON TECHNOLOGY

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ABSTRACT

The number system use in binary requires large number of interconnect which occupy around seventy percent area on an integrated chip. This limitation of area is reduced by using multi value logic number system. The two logic number systems are available in multi value logic system i.e. ternary number system and quaternary number system. The circuit design using multi value system is more advantageous if it use with binary logic system. This can be done by using binary to multi value logic conversions. The decimal systems starting states are use in binary, ternary, quaternary, cotal, hexadecimal number system. Other than these number system there are senary, duodecimal, quodradecimal and vigesimal number systems are use in MVL. The number system segmented the voltage level according to the number of states in MVL system.

Keywords: Multivalue Logic, Adder Implementation, Number System, High Radix

I. INTRODUCTION

A digital system operates on binary number system. the number system use in digital circuits are binary number system instead of using decimal number system. Other than this binary number system various other number systems are also use the fundamental concept of ten digit decimal number system. These numbers are ternary, quaternary, senary, Octal, duodecimal, quodradecimal, hexadecimal and vigesimal. The ternary number uses first three decimal number, quaternary uses first four decimal number, senary uses first six decimal numbers, octal uses first eight decimal numbers, duodecimal uses twelve, quodradecimal

Uses fourteen and hexadecimal uses sixteen decimal number system along with alphabetical characters.

In binary the number system the two voltage level indicates the one binary bit i.e. logic '1' and logic '0'. The voltage level 0V represents the binary logic '0' and the voltage level of 5V represents binary logic '1'. While the ternary logic number system uses three voltage levels of 0V, Vdd/3 and Vdd V, whereas the quaternary number system represents the four voltage levels of 0V, Vdd/2, 2Vdd/3, Vdd V. This voltage level may differ for both ternary and quaternary logic system. The encoder and decoder circuits are to convert binary logic to multi valued logic and multi valued logic to binary logic. The number system logic in ternary uses logic 0,1 and 2 while the quaternary number system uses logic 0,1,2 and 3.

II. TERNARY/QUATERNARY LOGIC LEVEL

One can achieve a more cost-effective way of utilizing interconnections by using a larger set of signals over the same area in multiple valued logic (MVL) devices, allowing easy implementation of circuits. In MVL devices,

the noise advantage of binary logic is retained. The higher radix in use is the ternary (radix-3) and the quaternary (radix-4). Two logic systems are available in ternary logic, balanced ternary logic -1, 0 and 1 and simple ternary logic 0, 1 and 2. The quaternary logic uses 0, 1, 2 and 3 logic levels. Figure 1 shows ternary logic with a voltage level. Figure 2 shows quaternary logic levels with voltage level.
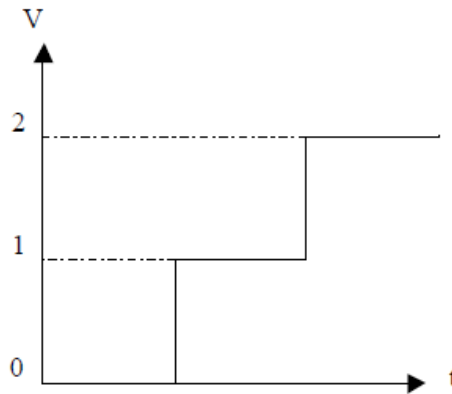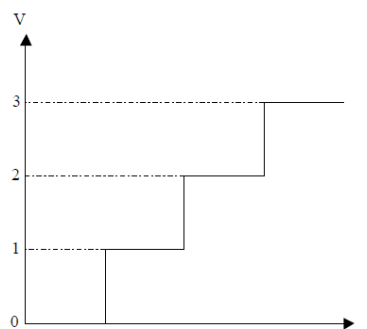

Figure 1. Ternary logic

Figure 2. quaternary logic levels

III. NUMBER SYSTEM INTERCONVERSIONS

The human being use decimal number system while computer uses binary number system. Therefore it is necessary to convert decimal number into its binary equivalent while feeding number into the computer and to convert binary into its decimal equivalent while displaying result of operation to the human beings. However, dealing with a large quantity of binary number of many bits is in convenient for human beings, therefore, octal and hexadecimal numbers are used as shorthand means of expression large binary numbers. But it is necessary to keep in mind that the digital circuits and systems work strictly in binary. Here this work proposes ternary and quaternary number system which is use for the circuit design of multi value logic. The octal and hexadecimal

only as a convenience for the operators of the system before going to see conversions between binary, octal and hexadecimal numbers we see the number of digits in several number systems. The number system whose radix is greater than 10 uses the alphabetic characters in their number system. For the arithmetic and logical operation and design of digital devices using these number systems it is very necessary to understand the structure of

number systems and its interconversions. For the arithmetic and logical operation and design of digital devices using these number systems it is very necessary to understand the structure of number systems and its interconversions. In this work the concepts of the mainly common number systems, their representation, arithmetic and logical, compliments and inter conversion is consider. It will present an simple understanding and practising of these number systems to know as well as memorise them.

IV. MVL HALF ADDER

The addition of two quaternary input signal through half adder logic is shown in the schematic. The transmission gates are use to design MVL half adder. The binary to quaternary converter is use to generate the MVL input of this adder circuit. Total 36 transmission gates, 24 inverter are required to design this adder circuit. These transmission gate and inverter requires 120 transistor for design.
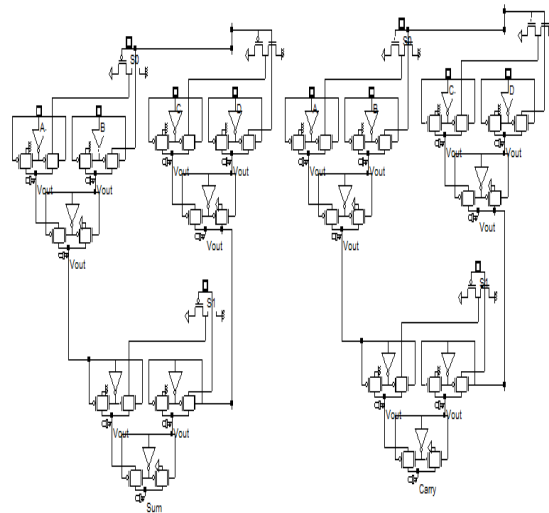

Figure 3. Half adder circuit

A half-adder is an arithmetic circuit block that can be used to add two bits. Such a circuit thus has two inputs that represent the two bits to be added and two outputs, with one producing the SUM output and the other producing the CARRY.

V. MVL FULL ADDER

A full-adder is an arithmetic circuit block that can be used to add three bits. Such a circuit thus has three inputs that represent the three bits to be added and two outputs, with one producing the SUM output and the other producing the CARRY. The addition of three quaternary input signal forms the SUM output is shown in the schematic. The transmission gates are use to design MVL full adder. The binary to quaternary converter is use to generate the MVL input of this adder circuit. Total 72 transmission gates, 48 inverter are required to design this adder circuit. These transmission gate and inverter requires 240 transistors for design.
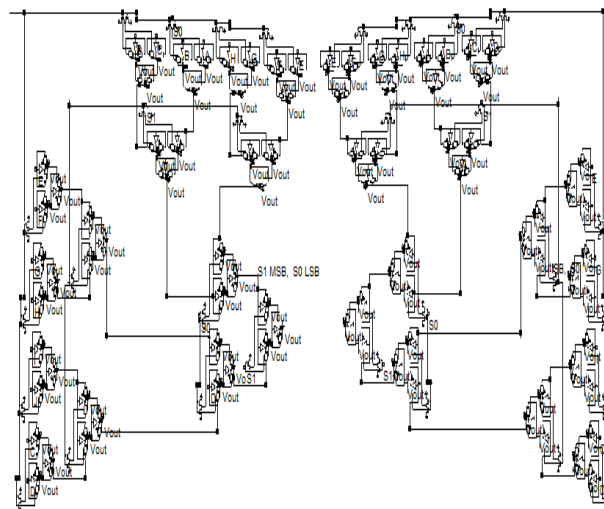
Figure 4. Sum Logic of MVL Full adder circuit

VI. RELATED WORK REVIEW

In [1] the quaternary 16 X 1 multiplexer logic design using transmission gate on 130nm technology with maximum supply voltage of 1.2V. The maximum power consumption of this work was 122uW. The architecture is base on switch like structure of transmission gate but is not immune to noise in circuit. They work on delay, area and energy consumption constraint in IC design using Quaternary Logic. A rise and fall delay calculates up to ps range for 16X1 multiplexer using quaternary logic circuits. The required logic to perform the shifts and to decode is design using quaternary to binary converters and look up tables. These blocks are implemented keeping area and energy consumption as low as possible while satisfying the delay constraints. Moreover, to convert the quaternary variable into binary, they added a comparator CP and an inverter to the comparators frontend, this extra block represented an increase of 5% on the QLUT area. This decoder is based on voltage-mode self-referenced comparators that allows the use of a standard CMOS technology and overcomes previous design drawbacks. Also, a CB technique was used to decrease the switches resistance and increase the operation frequency, while at the same time, achieving low power consumption. Therefore, the presented design is a valid solution to reduce the interconnections impact, without increasing power consumption or losing performance. But there design requires excessive number of transistors for their design.

In [2] multi value logic gates was design on 0.35 um technology for maximum 2.2V power supply. The logic levels are design for 0V, 0.7V, 1.4V and 2.2V voltage supply. The operators: extended AND (eAND1, eAND2, eAND3, Successor (SUC), and Maximum (MAX) have been implemented to illustrate the design of any Multiple-Valued Logic (MV Logic) digital circuit. A voltage CMOS divider is designed to set the logic voltages in the output. It obtains the maximum power consumption, from all possible logic conditions. For measuring the power consumption, a resistor was added between the source voltage and the IC source pin. They get power consumption in the range of 721uw to 1370 uW and the delay in the range of 30ns to 550ns.

In [3] multivalve logic base 2-digit modulo-16 up counter is design on micrometer technology. For this author design the pass transistor base current mode latch and flip-flop circuit. But their design needs improvement in circuit level, power dissipation, speed and extended system level design.

In [4] Quaternary to binary and binary to quaternary converters are designed on schematic level on Hspice simulator tool. Author design the Hspice code for multiplier, adder, subtraction circuit for multi threshold voltage transistor with) altering the width to length ratio of CMOS transistors, by ii) using pad MOS transistors and by iii) using multi threshold CMOS transistors..

In [5] the quaternary logic circuit base sign arithmetic logic is presented on micrometer technology level. For this they require three extra logical states. The converter circuit using operational Amplifier (OPAMP) is design which consists of n-channel MOS transistor having a gate electrode, which is electrically floating which is less tolerable for radiations.

In [6] the ternary logic base circuit is design. The resistance of channels can be change by altering the length-to-width ratio of the PMOS and NMOS channels. Thus, the resistance of the circuit is directly proportional to its L/W ratio which can be effectively used to change the resistance of transistors to suit design needs. On the other hand, there is a lower limit to the value of L and W due to the limitations imposed by the design rules of the foundry [6]. The proposed designs have much lower power dissipation relative to other known ternary circuits reported in the literature [6].

In [7] the multi-valued logic design consisting of two drivers and a transistor matrix was simulated on Mentor Graphic software. Its timing analysis for four levels of voltages i.e. 0V, 1.0V, 1.63V and 2.5V is simulates on this mentor graphic tool.

Therefore, despite the truth that decimal arithmetic is generally inferior to binary arithmetic; the need for decimal arithmetic still persists. Remember that the arithmetic operations such as addition, subtraction, multiplication and division of decimal numbers can be performed on all the numbers (such as binary, quaternary, senary, octal and so forth) as well. Therefore, in this section of the paper only the decimal arithmetic is described. However, the lower base system's arithmetic is much simpler than all the other number system's arithmetic, because these systems have fewer digits.

Related work Literature Review:

The design constraints in VLSI circuits are the major concern of integrated chip (IC) design. The design constraints includes speed, power, area, fan in, fan out and complexity of circuits. The complexity of circuits is mainly increases due to interconnect use in design. In the binary systems more data information requires more interconnects for design. The related work literature shows that the use of multi value circuits will reduce the number of interconnects which in turn reduces the cross talking in interconnects results in power dissipation minimization. The resistance and capacitance of contacts and interconnecting lines are currently a practical limitation on scaling of minimum geometries. Let the resistance and capacitance per unit length in the interconnections is R and C, respectively.

VII. CONCLUSION

In this work the number system base on the fundamental concept of decimal number system and its equivalent other number systems is discuss. The arithmetic addition of ternary and quaternary number system is similar to that of decimal addition. Digital circuit design is possible by using ternary and quaternary number system is

possible to design. But the digital circuit using other number system is not mostly design because the voltage levels use for this number system operates below the threshold voltage of transistor. =

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