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COMPARISON OF LOW POWER SCAN CHAIN ARCHITECTURES

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ABSTRACT

The testing power is the biggest concern in modern VLSI chip testing as the testing power is very greater than the functional power which affects the reliability of the chip. In this paper three different low power scan architectures are compared and power analysis has been done. The circuits are simulated in Cadence tool in 180nm technology.

Keywords :Linear Feedback Shift Register(LFSR),Serial In Serial Out(SISO),Parallel In Parallel Out(PIPO).

I. INTRODUCTION

The main objective of testing is to identify the number of defective chips due to manufacturing imperfection. The testing parameters considered during testing are test time, test power and fault coverage. In order to test the circuit every node has to be observable and controllable. The most widely used DFT technique is scan based design technique.

Power dissipation in CMOS is becoming a critical parameter during manufacturing test. The main sources of power dissipation are Static and Dynamic power dissipation. As all the components in the chip are active during test, the chip consumes much more power during testing than functional mode of operation. The major power sources in scan based design are the shift power and the capture power. In this paper three different low power architectures namely Illinois architecture [2], Broadcast architecture [2] and Segmented Broadcast architecture [1] have been compared. The rest of the paper is organized as follows, section II discuss the different Scan chain techniques that is being compared. Section III presents the modules used in scan architectures. Section IV deals with experimental results and analysis. Section V concludes the paper.

II.SCAN CHAIN ARCHITECTURES

A. Illinois scan architecture

Broadcast scan for multiple scan chains that drive the same circuits results in the loss of fault coverage due to the structural dependences in chains. The Illinois scan architecture deals with these dependences by utilizing two modes of operation; the broadcast mode and the serial mode [2]. Figure 1 shows the basic structure of the Illinois scan architecture. Parallel chains are connected into a single scan chain in a serial mode..

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Illinois Scan Architecture [6] (ISA) was initially proposed as the Serial Parallel Full Scan (SPFS) Architecture. It has been observed that it has remarkably lower test application time compared to any normal full scan architecture. Apart from this, there is a significant reduction in the amount of test data required for full scan embedded cores. The success of broadcasting methods depends on the ratio of the test patterns that can be broadcasted. They have been widely adopted by the industry. Several techniques were developed to deal with dependences, however the serial mode is used in most of them. Our aim is to develop a new test method based on the pattern overlapping and broadcasting. This new method would significantly reduce the test application time a test data volume and not impose large design overhead and complex control logic.

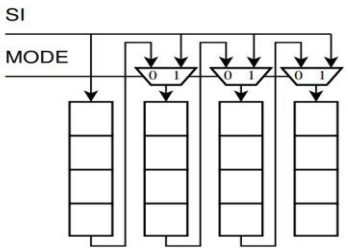

Fig. 1. Illinois scan architecture

B. Broadcast architecture

The broadcast architecture [2], is based on the Illinois scan. Fig 2 represents the architecture. In the Illinois scan there is generally a single fan- out stem that drives all scan chains with the data, There are dependences across the parallel chains because the corresponding scan cells across the parallel chains have the same data, as shown in Fig 1. The architecture consists of one source scan chain and multiple parallel scan chains. The source scan chain is not connected to a CUT, it just drives the parallel chains. There are also dependences across the parallel chains, however they are not across the corresponding scan cells but they are on the scan cells forming diagonals.

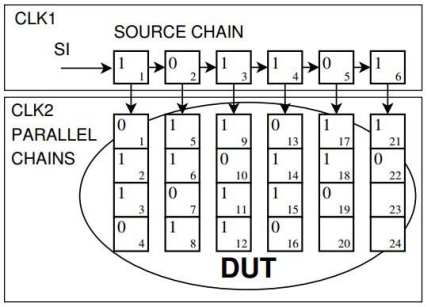

Fig. 2. Broadcast architecture

C. Segmented Broadcast architecture

In Segmented broadcast Architecture [1] shown in fig 3, the first scan chain and last scan chain is segmented into K segments and the patterns are loaded parallel into each segments [4]. The last scan flops are constructed with different mux called dual muxed scan flop as shown fig 4. Here the output of preceding flop in the same chain and the output of the flop from the previous chain are the inputs, this is because the response from all the scan chains are copied serially to the last chain and shifted out.

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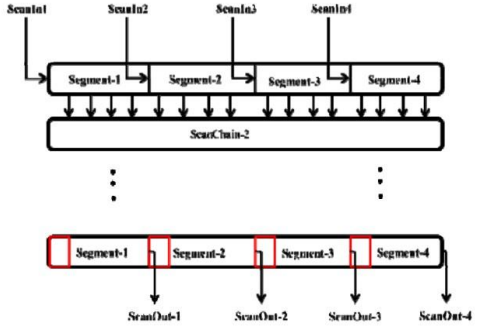

Fig. 3. Segmented Broadcast architecture

The values from the first scan chain are copied into the second scan chain parallely for this general scan chain structure in which the scan chains are connected in shift register fashion should be broken and connected in such a way that the scan out of the first flop of the first scan chain is connected to scan input of first flop of second scan chain this allows as to copy the pattern from one chain to other, the same structure is built for all flops between adjacent scan chains. If this structure is used with Illinois scan architecture the extra cycles will be double of number of scan chains [3].

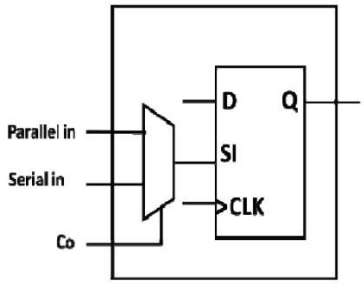

Fig. 4. Dual muxed scan flop

III. SIMULATION RESULTS AND MODULES OF SCAN ARCHITECTURES

A. LFSR

A linear-feedback shift register (LFSR) is a shift register whose input bit is a linear function of its previous state. The most commonly used linear function of single bits is exclusive-or (XOR). Thus, an LFSR is most often a shift register whose input bit is driven by the XOR of some bits of the overall shift register value. The simulated result is shown in fig 5.

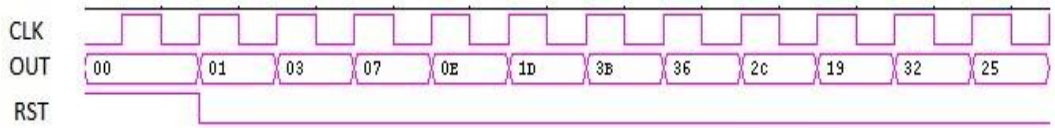

Fig. 5. LFSR Output

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B. SISO

A Serial In Serial Out (SISO) shift registers are a kind of shift registers where both data loading as well as data retrieval to/from the shift register occurs in serial-mode. A 4-bit synchronous SISO shift register sensitive to positive edge of the clock pulse. Here the data word which is to be stored is fed bit-by-bit at the input of the first flip-flop. The blocks required and the simulated results are shown in fig 6 and fig 7 respectively.

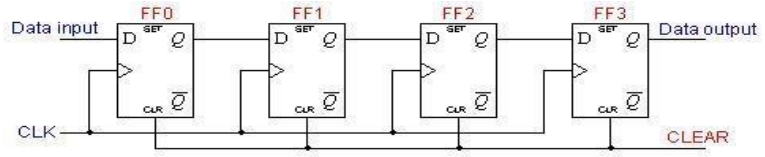

Fig. 6. SISO Block Diagram

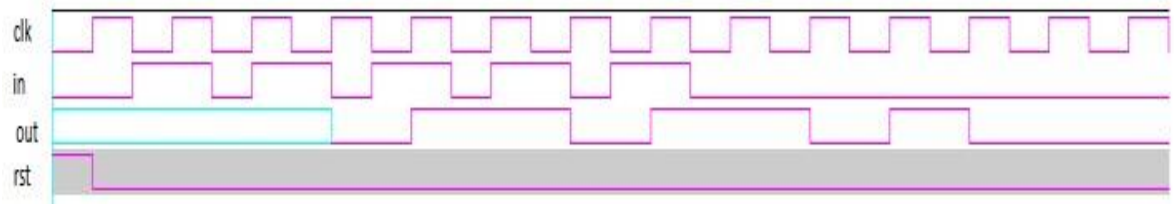

Fig. 7. SISO Output

C. PIPO

Parallel In Parallel Out (PIPO) shift registers are the type of storage devices in which both data loading as well as data retrieval processes occur in parallel mode. A PIPO register capable of storing 4-bit input data word (Data in).Each flip- flop stores an individual bit of the data in appearing as its input at the instant of first clock pulse. The blocks required and the simulated results are shown in fig 8 and fig 9 respectively.

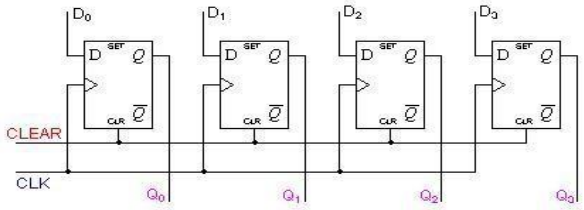

Fig. 8. PIPO Block Diagram

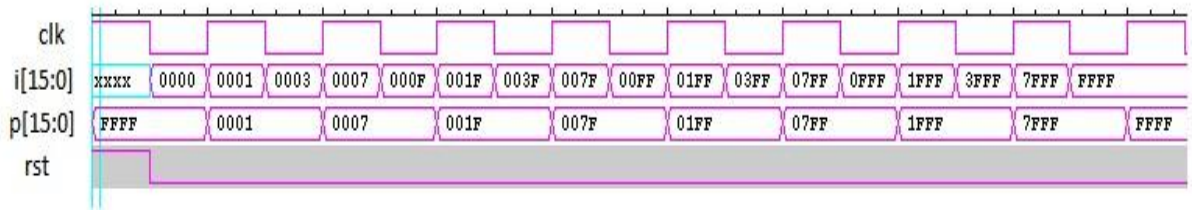

Fig. 9. PIPO Output

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D. DUAL MUXED SCAN FLOP

In muxed scan flop the output of preceding flop in the same chain and the output of the flop from the previous chain are the inputs, this is because the response from the entire scan chains are copied serially to the last chain and shifted out. The simulation result is shown in fig 10.

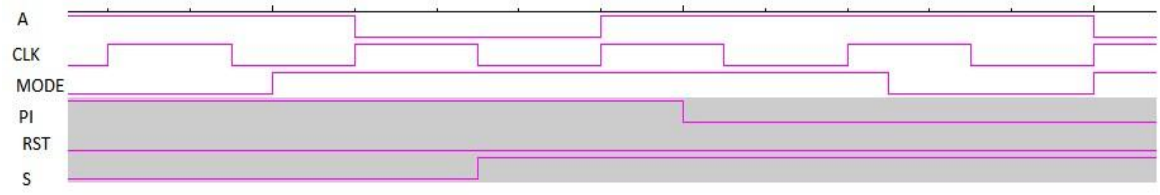

Fig. 10. Muxed scan flop output

IV. RESULTS AND DISCUSSIONS

A. ILLINOIS ARCHITECTURE

The RTL schematic and simulation results of Illinois scan architecture is shown in Fig 11 and Fig 12.

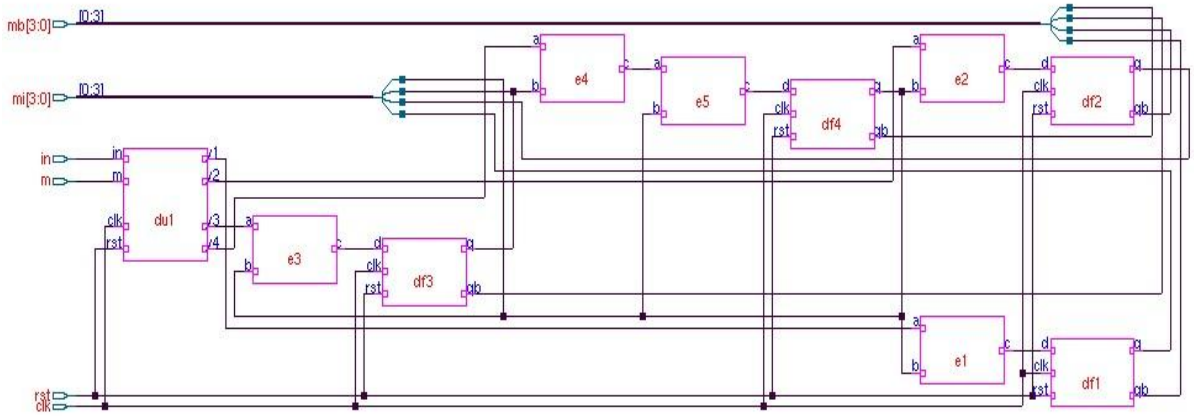

Fig. 11. Illinois Scan Chain RTL

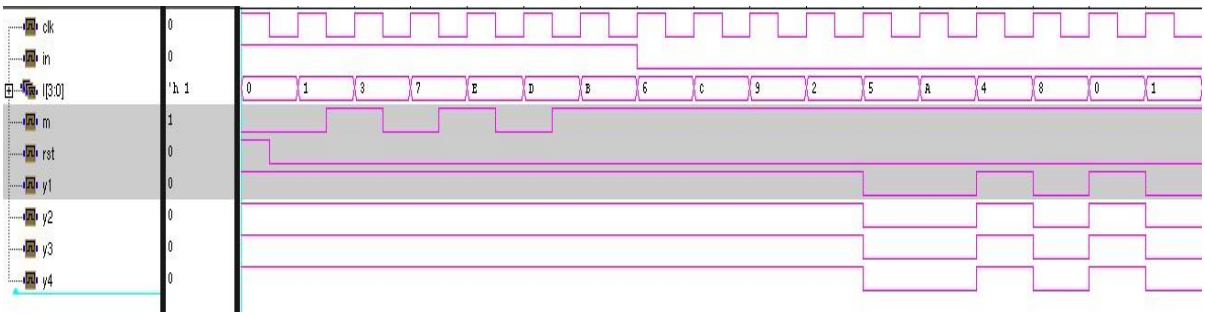

Fig. 12. Illinois Scan Chain Output

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B. BROADCAST ARCHITECTURE

The RTL schematic and simulation results of Broadcast Architecture is shown in Fig 13 and Fig 14

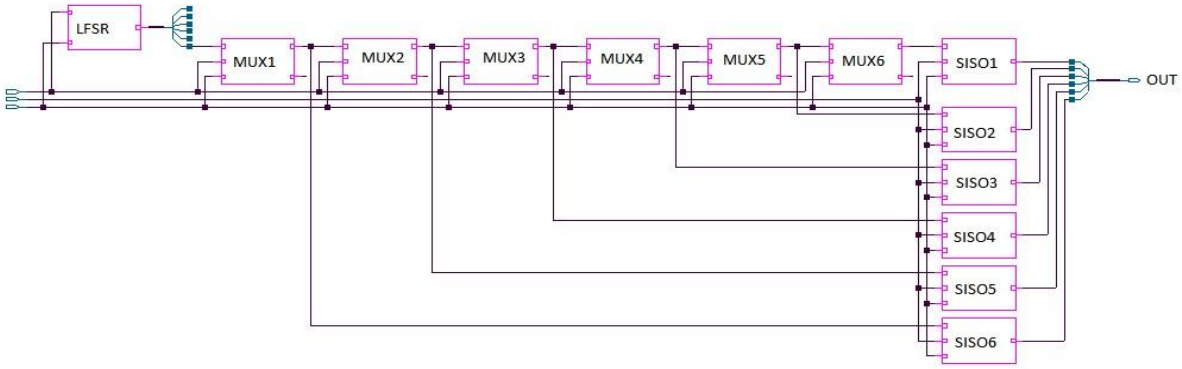

Fig. 13. Broadcast Architecture RTL

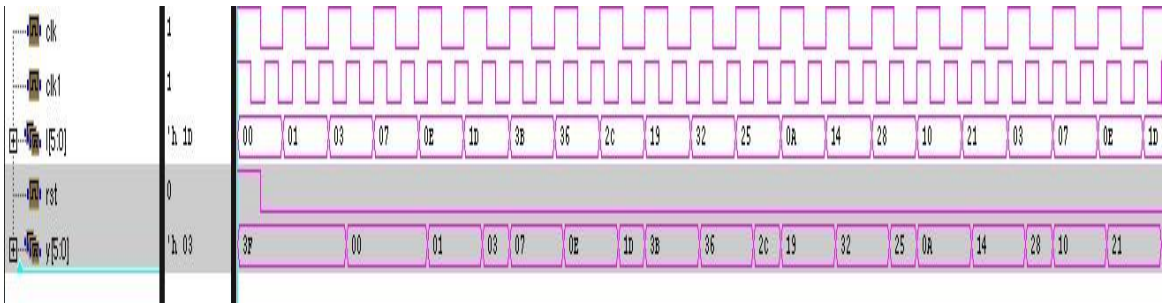

Fig. 14. Broadcast architecture Output

C. SEGMENTED BROADCAST ARCHITECTURE

The RTL schematic and simulated results of Segmented Broadcast Architecture is shown in Fig 15 and 16

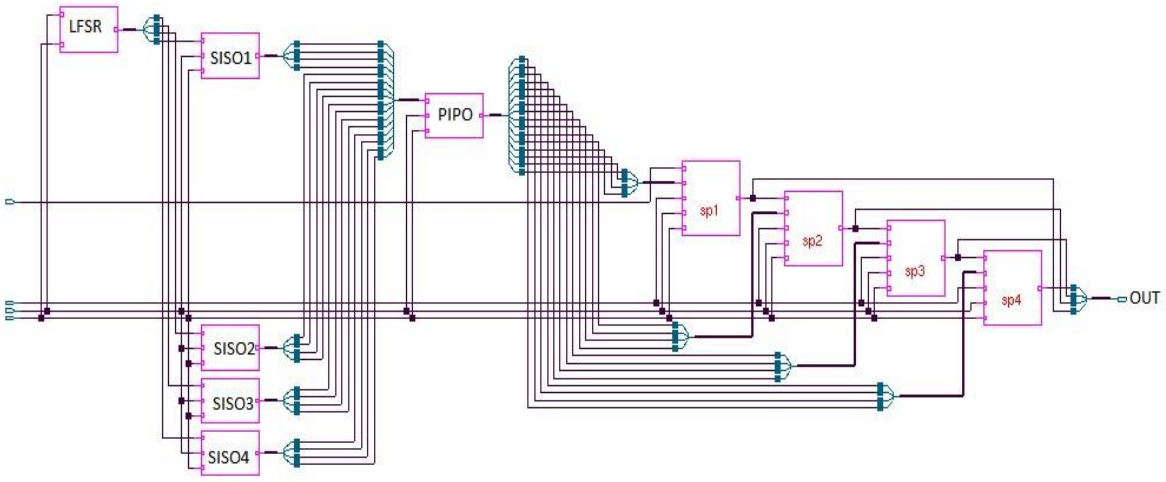

Fig. 15. Segmented Broadcast architecture RTL

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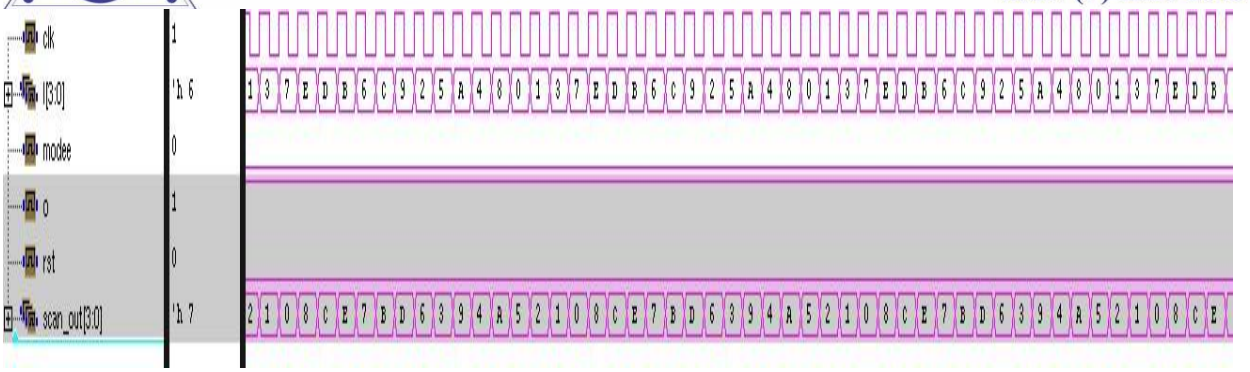

Fig. 16. Segmented Broadcast Architecture output

D. COMPARISON OF POWER RESULTS

POWER	ILLINOIS ARCHITECTURE	BROADCAST ARCHITECTURE	SEGMENTED BROADCAST ARCHITECTURE
LEAKAGE (nW)	51.466	32.913	51.466
DYNAMIC (nW)	437434.545	249236.842	146433.545
TOTAL (nW)	437486.011	249269.756	146485.011

Table I. Results of Power dissipation in discussed Architectures

The comparison of power dissipation of the three architectures has been achieved using Cadence 180nm technology. The Static (leakage) power of Segmented Broadcast Architecture is same as that of Illinois architecture and greater than Broadcast Architecture. But the dynamic power is lesser than both. Hence total power dissipation in Segmented Broadcast Architecture is very less when compared with other two architectures.

V. CONCLUSION

In this paper different low power scan architectures are compared and the best low power architecture is found which reduces the testing power in the scan based design. The Segmented Broadcast Architecture technique is more power efficient than Illinois and Broadcast architecture where the scan chains are segmented and feed with test pattern in parallel fashion. All the three architectures are built in CADENCE tool with 180nm technology.

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