International Journal of Electrical and Electronics Engineers
Vol. No. 9, Issue No. 02, July - December 2017
ISSN (O) 2321-2055
ISSN (P) 2321-2045

Design and Implementation of ALU using GDI Technique

D.Vigneshwari

Assistant Professor, ECE Dept, Dhruva Institute of Engineering & Technology, (India)

ABSTRACT

Low power and area efficient design has become one of the prime focus for the digital and analog VLSI circuit. The purpose of this paper is to design low power and area efficient ALU using GDI technique. Main sub modules of ALU are adder, logical unit, comparator, one's complement, multiplexer. This work evaluates and compares the performance & optimized area of ALU with conventional CMOS style & GDI technique the simulations are performed by using cadence EDA tool in 180 nm technology. At first by using cadence virtuoso tool the circuits are designed &simulated with CMOS technique and then with GDI technique.by comparing two designs GDI & CMOS style then GDI is an advantage of less power and less area.

Keywords*: *ALU, GDI, Adder, Comparator, logical unit, 1's complement, multiplexer, low power.

I. INTRODUCTION

Recently, the industries are demand for low power, less area and high speed for designing the circuits. With improvement in technology and the enlargement of embedded system used electronic devices such as mobile,laptops,TV applications, power consumption, which is one of the limits in both high & low performance system, has become a primary focus in VLSI digital design.

In this paper the adder was based on regular CMOS structure (pull-up and pull-down network) [1]. Disadvantage of this paper is but the uses a number of transistors results inmore power consumption ,high input loads and larger silicon area.

Morgenshtein has proposed basic GDI cell[4].By using this GDI cell we design ALU. In digital system design processor is main part of the system. And an ALU is one of the main components of a micro-processor. CPU works as a brain to any system & and ALU works as a brain to CPU. So it's a brain of computer's brain. They consists of fast dynamic logic circuits and have carefully optimized structures. Of total power consumption in any processor, CPU accounts a significant portion of it. Therefore, this motivate us strongly for a energy-efficient ALU designs that satisfy the high-performance requirements, while reducing power dissipation.In combinational circuits alu is one of the most important circuit that performs arithmetic operations and logical operations e.g. A [0:3] & B [0:3] for 4 bits. The internal structure of a ALU is shown in Fig.1.

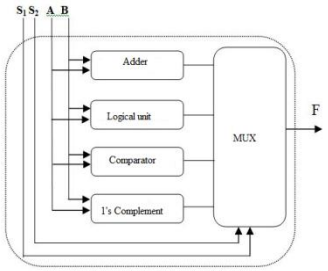

Fig. 1. Internal architecture of ALU

The rest of paper is organized into these Section II describes description of ALU. Section III consisting of designing of various ALU components such as comparator, adder, subtractor etc. using conventional CMOS.Section IV presents the ALU using GDI technique Section V describes simulation result and analysis. At last conclusion is made in section VI.

II . DESCRIPTION OF ARITHMETIC LOGICAL UNIT

In central processing unit (CPU) arithmetic logical unit (ALU) is a crucial component.it does all arithmetic logical operations and logical operations.The ALU is divided into the arithmetic unit (AU) and the logic unit (LU).

2.1 Arithmetic Unit

Arithmetical operations are performed by using ALU. Arithmetical operations are addition, subtraction, multiplication etc.in this project. Fast and efficient adders in arithmetic logic unit will aid in the design of low power. Different adders aredesign in past to reduce the power, area and increase the speed.

2.2 Logic Unit

ALU can perform different logical operations that are AND, OR, NOT, NAND, NOR, EXOR, EXNOR etc. This logical operations are performed

2.3 Comparator

In digital systems comparator is a basic arithmetic component. comparator compare the input values and produce the three out puts these are equal (A=B) less than condition (A<B), greater than (A>B)[2].when two inputs A,B are same values then it produces ‘e’ output ,if A value is higher than B value the output is ‘g’ else it produces output as‘l’.

2.4 ONE’S COMPLEMENT

By using one’s complement we can perform the inversion operation of the input. One’s complement perform by using NOT gate. NOT gate works like this if 1 is input then output is 0 else output is 1.

MULTIPLEXER

Multiplexer is a combinational circuit that select several digital or analog input signal and forward the selected input into a single output line. Multiplexer is also called as data selector.in this project we use 4:1 mux. Sub modules are selected by multiplexer.

III ALU COMPONENTS DESIGN BY USING CMOS.

By using CMOS(complementary metal oxide semiconductor) technique The various components are designed. Figure shows the schematic design of various components such as ADDER, COMPARATOR, 1’S COMPLEMENT, and LOGICAL GATES.

International Journal of Electrical and Electronics Engineers
Vol. No. 9, Issue No. 02, July - December 2017
ISSN (O) 2321-2055
ISSN (P) 2321-2045

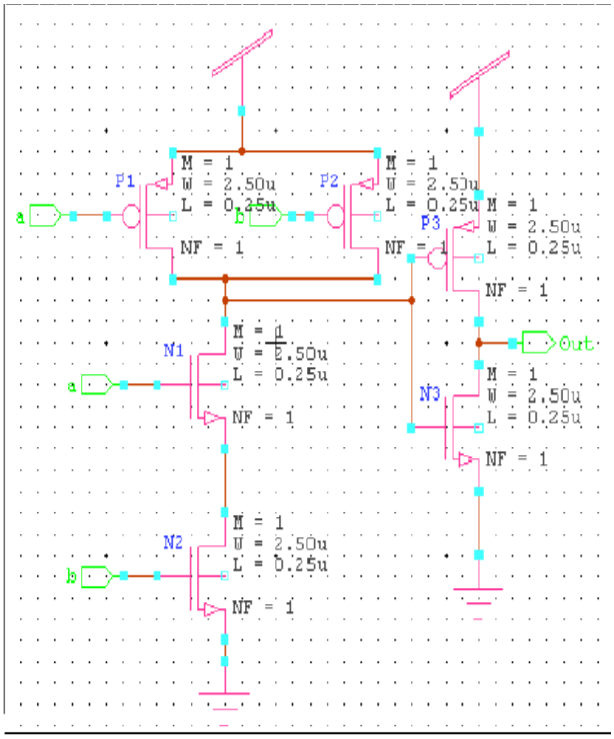

Fig AND gate schematic using CMOS

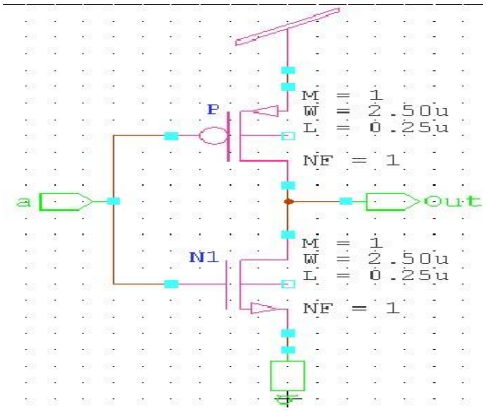

Fig Inverter using CMOS

Sr.no	Input			Output	Function
	G	P	N		
1	A	B	0	$\overline{A}.B$	F1
2	A	1	B	$\overline{A}+B$	F2
3	A	B	1	A+B	OR
4	A	0	B	A.B	AND
5	A	B	C	$\overline{A}.B+AC$	MUX
6	A	1	0	$\overline{A}$	NOT

International Journal of Electrical and Electronics Engineers
Vol. No. 9, Issue No. 02, July - December 2017
ISSN (O) 2321-2055
ISSN (P) 2321-2045

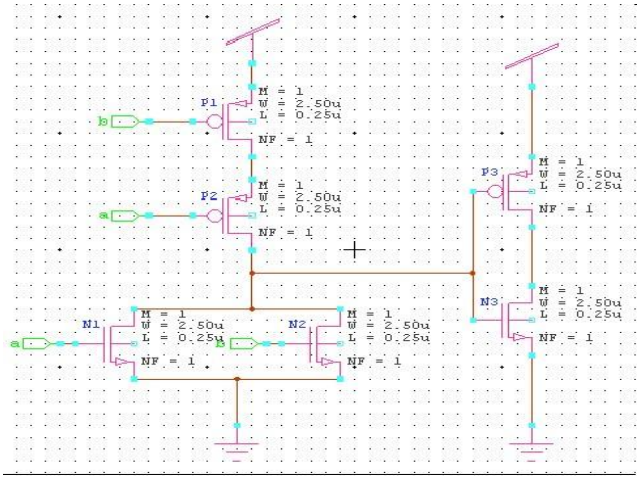

Fig OR gate using CMOS

Mostly all other circuits are design by using this threeCircuits AND, OR, NOT. using thecmos logic result in high power consumption and it requires a more number of.Transistors.so inorder toreducethe power consumptionand less number of transistorthe proposedsystem is designed. that proposedis GateDifu

sion Input(GDI) technique.

IV. PROPOSED GDI ALU

Morgenshtein has proposed basic GDI cell [4].The GDI cell fig is shown in below.GDI cell design by using one PMOS,one NMOS transistor.It is same as CMOS inverter but only differences is two

1).First onesis it having three inputs pins ,these are G,P,N and one out pin is out

- Input pin G is common gate of PMOS and NMOS.
- Input pin P is input to the source/drain of PMOS.
- Input pin N is input to the source/drain of NMOS.

2).Bulks of NMOS and PMOS are connected to N or P (re- spectively), so it can be arbitrarily biased in contrast to CMOS inverter

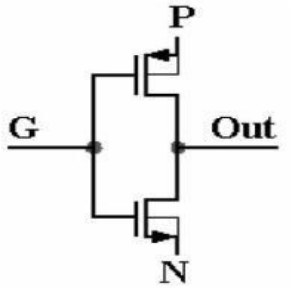

TABLE I: GDI cell functions

The basic GDI cell performs the below functions [4].the table is shown in below table I

International Journal of Electrical and Electronics Engineers
Vol. No. 9, Issue No. 02, July - December 2017
ISSN (O) 2321-2055
ISSN (P) 2321-2045

To design a 4 bit Adder circuit .The main block is fulladder,this full adder [1]design by using GDI technique is shown in below fig 5.It requires a less number of components compare to CMOS design.

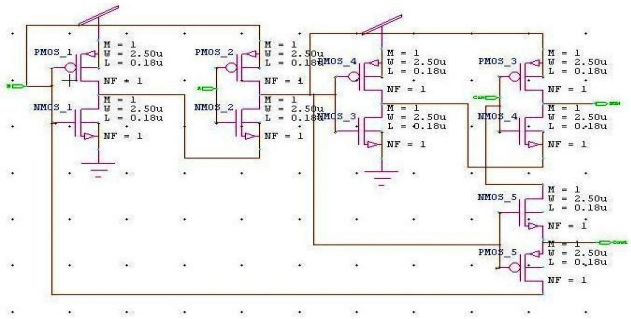

Fig 5 full adder schematic using GDI technique

V. SIMULATION AND RESULTS

This section describes the proposed alu is design using virtuoso tool on 180nm technology. The simulated out puts of both designs proposed and existing designs output are shown in below.

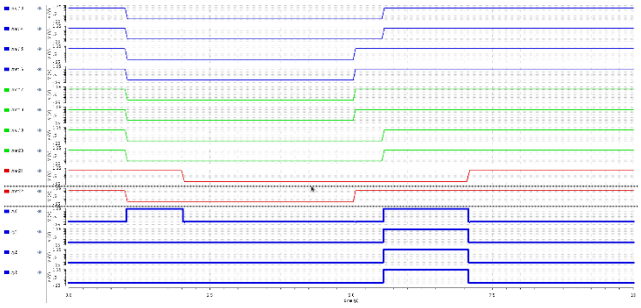

Fig 5:Wave Forms Of 4 Bit ALU Using CMOS

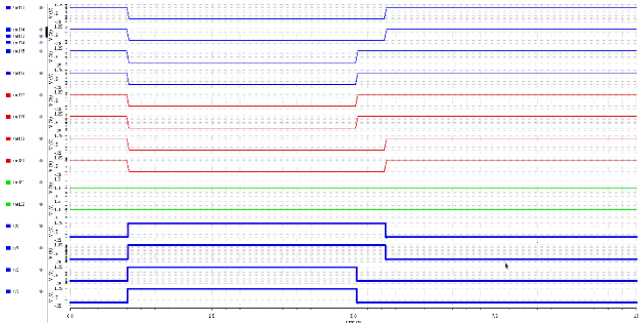

Fig 6: Wave forms of 4 bit ALU using GDI

The number of transistor required and power consumption for the sub-modules of the ALU is listed in below tableII

S.No	Module	No. of Transistors		Power(Watts)	
		CMOS	GDI	CMOS	GDI
1	Adder	120	60	95.10E-6	60.67E-6
2	AND gate	24	8	70.94E-6	55.83E-6
3	Comparator	160	90	443.2E-6	422.36E-6
4	1's complement	8	8	50.31E-6	35.92E-6
5	Multiplexer	96	50	380.9E-6	330.5E-6
6	ALU	360	196	500.1E-6	430.8E-6

TABLE: Comparison of Power and No of Transistor Used by GDI & CMOS

VI. CONCLUSION

In this paper, conventional CMOS technique for the designing of ALU is discussed first. A lowpower and area optimizing technique is introduced and the components with this technique are implemented. Later the comparison between thenumber of transistor used in CMOS and GDI design of ALU is done. And in the results is shows that this GDI design is reduces the power and the number of transistor and hence optimize the area of ALU as well increase its working speed.

REFERENCE

[1] R. Shalem, E. John, and L.K. John, proposed a conventional CMOS full adder consisting of 28 transistors.

[2] Arun Prakash Singh, Rohit Kumar, ―Implementation of 1-bit Full Adder using Gate Diffusion Input (GDI) cell , International Journal of Electronics and Computer Science Engineering, ISSN- 2277-1956/V1N2-333-342.

[3] VijayaShekhawat,Tripati,KrishnaGopal Sharma,-2 bit magnitude comparator using GDI Technique.

[4] ArkadiyMorgenshtein, Alexander Fish, and Israel A. Wagner, ―Gate-Diffusion Input (GDI): A Power-Efficient Method for Digital Combinatorial Circuits , IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 10, No. 5, October 2002.

[5] VaibhavNeema, Pratibha Gupta, ―Design Strategy for Barrel Shifter Using Mux at 180nm Technology Node , International Journal of Science and Modern Engineering (IJISME), ISSN: 2319-6386, Volume-1, Issue-8, July 2013.

[6] Shrivastava, A.; Kannan, D.; Bhardwaj, S. Vrudhula, Reducing functional unit power consumption and its variation using leakage sensors, IEEE transactions on very large scale integration (VLSI) systems, vol. 18, no. 6, pp.988-997, June 2010.

[7] Dan Wang, Maofeng Yang, Wu Cheng, Xuguang Guan, Zhangming Zhu, Yintang Yang, ―Novel Low Power Full Adder Cells in 180nm CMOS Technology , ICIEA 2009, 978-1-4244- 2800-7/09/$25.00 ©2009 IEEE.