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Performance Analysis of a Low-Power High Speed Hybrid Full Adder Circuit

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ABSTRACT

Now performance of DSP processors are calculated based the design of Adders. Since Adders are basic built blocks for ALU design. SO many low power low area design are introduced. SO in this paper we show a hybrid design of Full adder which generates the high logic outputs. Then we introduces a new GDI design of Full adder with high Swing outputs as well less area, these circuit simulation was carried using Tanner EAD tool.

Keywords: Adders, Hybrid CMOS, GDI, Tanner EDA.

I. INTRODUCTION

Due to rapid advances in electronic technology, electronic smarket is becoming more competitive, which results in consumer electronic products requiring even more stringently high quality. The design of consumer electronic products requires not only light weight and slim size, but also low power and fast time-to-market. Therefore, the integrated circuit (IC) designers have to consider more important issues such as chip area, power consumption, operation speed, circuit regularity, and so on. Due to these design issues relevant to the key competitive factors of electronic systems, IC designers and electronic design automation (EDA) vendor are very concerned about the development of effective methodologies to fetch smaller chip area design, lower power consumption, faster operation speed and more regular circuit structure The arithmetic circuit is the important core in electronic systems. If the arithmetic circuit has good haracteristics, the overall performance of electronic systems will be Improved dramatically. Obviously, the performance of the arithmetic circuit directly determines whether the electronic system in market is competitive. It is well known that full adder is the crucial building block used to design multiplier, microprocessor, digital signal processor (DSP), and other arithmetic related circuits. In addition, the full adder is also dominant in fast adder design. Therefore, to effectively design a full adder with smaller chip area, low power consumption, fast operation speed and regular circuit structure, are the common required for IC designers. Since full adder plays an extremely important role in arithmetic related designs, many IC designers puts a lot of efforts on full adder circuit research. Consequently, there are many different types of full adders have been developed for a variety of different applications. These different types of full adders have different circuit structures and performance.

Full adder designs have to make tradeoff among many features including lower power consumption, faster operating speed, reduced transistor count, full-swing output voltage and the output driving capability, depending on their applications to meet the needs of electronic systems. One important kind of full adder designs focus on adopting minimum transistor count to save chip area [1, 2, 3, 4, 5]. These full adder

designs with fewer transistors to save chip area does have excellent performance, however, due to MOS transistors reduced, these full adders have threshold voltage loss problem and poor output driving capability. Some full adders are designed to emphasize making up for threshold voltage loss to improve circuit performance [6, 7]. These full-swing full adder designs insist on using fewer MOS transistors to reduce circuit complexity to go along with reduced power consumption and delay time. However, the full-swing full adders have no output driver in design leading to signal attenuation problems when they are connected in series to construct multi-bit are increased circuit complexity, larger chip area, difficult layout design, and increased transistor count. Therefore, how to design a full adder circuit with better performance and simpler structure is the main goal of full adder design field. In order to design a full adder with low circuit complexity, good circuit performance and the modularized structures, a multiplexer- based full adder is proposed in this study. The multiplexer- based full adder has not only regularly modularized structure, but also superior circuit performance. The rest of this paper is organized as follows: In sectionII, some previous works on full adder design are discussed. A novel multiplexer-based full adder design is presented in sectionIII. In sectionIV, we show the experimental results and make a discussion. Finally, a brief conclusion is given in sectionV.

A. Previous Works on Full Adder Design

The full adder function is to sum two binary operands A, B and a carry input C_i, and then generate a sum output (S)and carry output (C_O). There are two factors affecting the performance of a full adder design: one is the full adder logic architecture, and the other is the circuit design techniques to perform the logic architecture function. Therefore, the full adder design approach requires using different types of logic architecture and circuit design technique to improve the total performance.

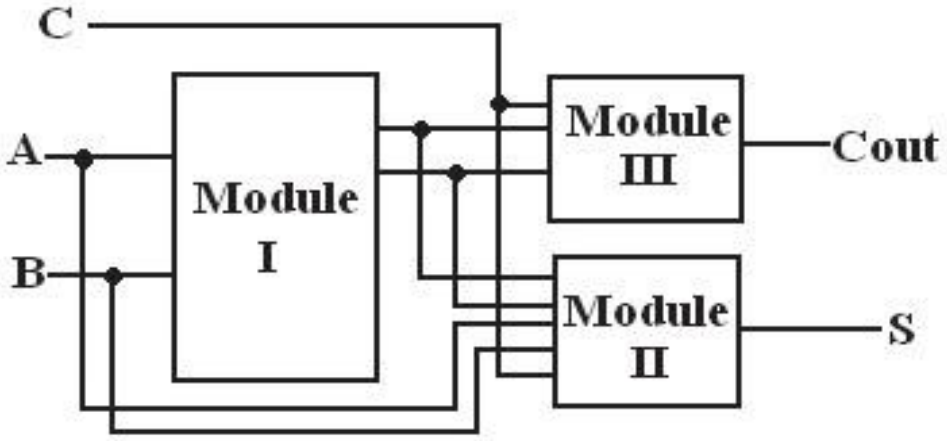

Fig.1. Full Adder Logic Architecture with Three Modules.

The traditional full adder logic architecture can be divided into three modules [6, 7,], and the logic architecture block diagram is shown in Fig. 1. Module I was designed using XOR/XNOR gate and Module II was designed using XOR gate and Module III was designed using Multiplexer. These three

modules are designed using Hybrid CMOS design style and using GDI techniques and their results are compared using Tanner EDA Tools.

II. DESIGN CONSIDERATIONS

A. Impact of Logic Style

The logic style used in logic gates basically influences the speed, size, power dissipation, and the wiring complexity of a circuit. The circuit delay is determined by the number of inversion levels, the number of transistors in series, transistor sizes[3] (i.e., channel widths), and intra- and inter-cell wiring capacitances. Circuit size depends on the number of transistors and their sizes and on the wiring complexity. Power dissipation is determined by the switching activity and the node capacitances(made up of gate, diffusion, and wire capacitances), the latter of which in turn is a function of the same parameters that also control circuit size. Finally, the wiring complexity is determined by the number of connections and their lengths and by whether single-rail or dual-rail logic is used. All these characteristics may vary considerably from one logic style to another and thus make the proper choice of logic style crucial for circuit performance. As far as cell-based design techniques (e.g., standard-cells) and logic synthesis are concerned, ease-of- use and generality of logic gates is of importance as well. Robustness1 with respect to voltage and transistor scaling as well as varying process and working conditions, and compatibility with surrounding circuitries are important aspects influenced by the implemented logic style.

B. Logic Style Requirements for Low Power

$$P_{dyn} = V_{dd}^2 \cdot f_{clk} \cdot \sum_n \alpha_n \cdot c_n + V_{dd} \cdot \sum_n i_{sc_n}$$

According to the formula the dynamic power dissipation of a digital CMOS circuit depends on the supply voltage the clock frequency , the node switching activities the node capacitances, the node short circuit currents and the number of nodes. A reduction of each of these parameters results in a reduction of dissipated power[4]. However, clock frequency reduction is only feasible at the architecture level, whereas at the circuit level frequency is usually regarded as constant in order to fulfill some given throughput requirement. All the other parameters are influenced to some degree by the logic style applied. Thus, some general logic style requirements for low-power circuit implementation can be stated at this point.

1. Switched Capacitance Reduction: Capacitive load, originating from transistor capacitances (gate and diffusion) and interconnect wiring, is to be minimized. This is achieved by having as few transistors and circuit nodes as possible, and by reducing transistor sizes to minimum. In particular, the number of (high capacitive) inter-cell connections and their length (influenced by the circuit size) should be kept minimal. Another source for capacitance reduction is found at the layout level [4], which, however, is not discussed in this paper. Transistor downsizing is an effective way to reduce switched capacitance of logic gates on noncritical signal paths [5]. For that purpose, a logic style should be robust against transistor downsizing, i.e., correct functioning of logic gates with minimal or near-minimal transistor sizes must be guaranteed (ratio less logic).

2. Supply Voltage Reduction: The supply voltage and the choice of logic style are indirectly related through delay-driven voltage scaling. That is, a logic style providing fast logic gates to speed up critical signal paths allows a reduction of the supply voltage in order to achieve a given throughput. For that purpose, a logic style must be robust against supply voltage reduction, i.e., performance and correct functioning of gates must be guaranteed at low voltages as well. This becomes a severe problem very low voltage of around 1 V and lower, where noise margins become critical.

3. Switching Activity Reduction: Switching activity of a circuit is predominantly controlled at the architectural and register transfer level (RTL). At the circuit level, large differences are primarily observed between static and dynamic logic styles. On the other hand, only minor transition activity variations are observed among different static logic styles and among logic gates of different complexity, also if glitching is concerned.

4. Short-Circuit Current Reduction: Short-circuit currents (also called dynamic leakage currents or overlap currents)may vary by a considerable amount between different logic styles. They also strongly depend on input signal slopes (i.e., steep and balanced signal slopes are better)[7] and thus on transistor sizing. Their contribution to the overall power consumption is rather limited but still not negligible (≈10–30%), except for very low voltages where the short-circuit currents disappear. A low-power logic style should have minimal short-circuit currents and, of course, no static currents besides the inherent CMOS leakage currents

C. Logic Style Requirements for Ease-of-Use

For ease-of-use and generality of gates,a logic style should be highly robust and have friendly electrical characteristics, that is, decoupling of gate inputs and outputs (i.e., at least one inverter stage per gate) as well as good driving capabilities and full signal swings at the gate outputs, so that logic gates can be cascaded arbitrarily and work reliably in any circuit configuration. These properties are prerequisites for cell-based design and logic synthesis, and they also allow for efficient gate modeling and gate-level simulation. Furthermore, a logic style should allow the efficient implementation of arbitrary logic functions and provide some regularity with respect to circuit and layout realization. Both low-power and high-speed versions of logic cells (e.g., by way of transistor sizing) should be supported in order to allow flexible power-delay tuning by the designer or the synthesis tool.

D. Static Vs Dynamic logical Style

A major distinction, also with respect to power dissipation, must be made between static and dynamic logic styles. As opposed to static gates, dynamic gates are clocked and work in two phases, a pre charge and an evaluation phase. The logic function is realized in a single NMOS pull-down or PMOS pull- up network, resulting in small input capacitances and fast evaluation times. This makes dynamic logic attractive for high- speed applications. However, the large clock loads and the high signal transition activities due to the precharging mechanism result in an excessive high power dissipation. Also, the usage of dynamic gates is not as straightforward and universal as it is for static gates, and robustness is considerably degraded. With

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the exception of some very special circuit applications, dynamic logic is no viable candidate for low-power circuit design

III. DESIGN TECHNOLOGIES

There are many sorts of techniques that intend to solve the Problems mentioned above

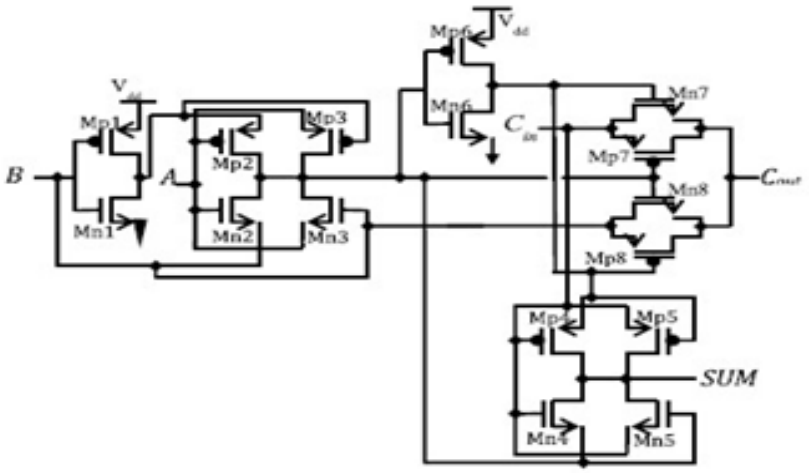

Fig.2. Hybrid CMOS Full Adder

A. Full Adder Design

So = H′Ci + HC′o (2)

Co = HCi + H′A (3)

where H = A Xor B and H′ = A Xnor B. An Full Adder is made up of an XOR–XNOR module, a sum module and a carry

module. The XOR–XNOR module performs XOR and XNOR logic operations on inputs A and B, and then generates the outputs H and H′. Subsequently, H and H′ both are applied to the sum and the carry modules for generation of sum output So and carry output Co.

B. Modified XNOR Module

Module I In the proposed full adder circuit, XNOR module is responsible for most of the power consumption of the entire

adder circuit. Therefore, this module is designed to minimize the power to the best possible extend with avoiding the voltage degradation possibility. Fig shows the modified XNOR circuit where the power consumption is reduced significantly by deliberate use of weak inverter (channel width of transistors

being small) formed by transistors Mp1 and Mn1. Full swing of

the levels of output signals is guaranteed by level restoring transistors Mp3 and Mn3 [Fig. (b)]. Various XOR/XNOR topologies have already been reported in [7] and [2]–[4]. The XOR/XNOR reported in [2]–[4]

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uses four transistors but at the cost of low logic swing. To the contrary, the XOR/XNOR reported in [7] uses six transistors to get better logic swing compared with that of 4 T XOR/XNOR [2]–[4]. In this paper also, the XNOR module employed 6 T, but having different transistor arrangement than that of 6 T XOR/XNOR [7]. The modified XNOR presented in this paper offers low-power and high-speed (with acceptable logic swing) compared with 6 T XOR/XNOR

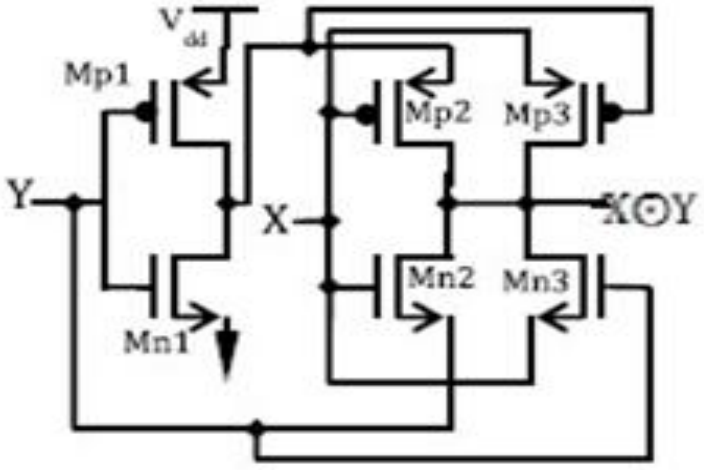

Fig.3. Module 1& III

C. Carry Generation Module

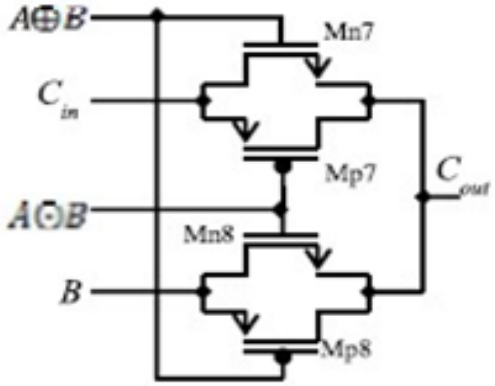

Fig.4. Carry Generation Block.

In the proposed circuit, the output carry signal is implemented by the transistors Mp7, Mp8, Mn7, and Mn8 as shown in Fig.

1(c). The input carry signal (*Cin)* propagates only through a

single transmission gate (Mn7 and Mp7), reducing the overall carry propagation path significantly. The deliberate use of strong transmission gates (channel width of transistors Mn7, Mp7, Mn8, and Mp8 is made large) guaranteed further reduction in propagation delay of the carry signal

D. Tabulation

The above circuits of full adder are simulated using Tanner Tools using 90nm and TSMC018 and its delay and power of individual circuits are tabulated.

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TABLE I. Simulation Results for Full Adders in 90nm Technology With 1.2v Supply

design	Power	Delay	PDP	Transistor count
CMOS	3.807	4.874	1.855	28
CPL	3.223	4.546	1.465	32
TFA	7.129	4.670	3.329	16
TGA	3.232	9.633	3.113	20
HPSC	3.023	4.587	1.386	22
24T	4.681	4.581	2.143	24
hybrid	4.091	4.379	1.843	24
mirror	4.069	4.292	1.746	28
proposed	2.661	4.278	1.138	16

TABLE II. Simulation Results for Full Adders in 180nm Technology with 1.8v Supply

design	power	delay	PDP	Transistor count
CMOS	**3.807**	**4.424**	**1.684**	**28**
CPL	**3.223**	**4.605**	**1.484**	**32**
TFA	**5.710**	**3.440**	**1.964**	**16**
TGA	**2.707**	**9.633**	**2.607**	**20**
HPSC	**6.729**	**3.683**	**2.478**	**22**
24T	**4.681**	**4.214**	**1.972**	**24**
HYBRID	**4.091**	**4.453**	**1.821**	**24**
Mirror	**5.166**	**4.292**	**2.217**	**28**
Proposed	**2.661**	**4.278**	**1.138**	**16**

TABLE III. Simulation Results for Full Adders in 90nm Technology with 1.2v Supply

Design	Power	Delay	PDP
8-CMOS	**8.156**	**5.120**	**4.175**
8-TGA	**3.954**	**4.984**	**1.984**
8-proposed	**2.776**	**5.033**	**1.397**
16-proposed	**2.329**	**5.038**	**1.173**

TABLE IV. Simulation Results for Full Adders in 180nm Technology with 1.8v Supply

Design	Power	Delay	PDP
8-CMOS	**3.530**	**5.120**	**1.807**
8-TGA	**5.221**	**4.984**	**2.602**
8-proposed	**2.716**	**5.038**	**1.368**
16-proposed	**2.329**	**5.038**	**1.173**

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TABLE V. Simulation Results for Applications with 90nm and 180nm Technology

Technology	Design	Powe	Dela	PDP
90nm	4-CLA	1.104	5.031	5.554
180nm	4-CLA	1.357	5.031	6.827

TABLE VI. Simulation Results for Applications with Ptm.22nm-Hk Technology

Desig	Powe	Dela	PDP
4-	6.976	6.75	4.710

IV. CONCLUSION

As the core of an arithmetic circuit, that is a key module in a large number of portable electronic systems, an High Speed Full Adders presented in this Letter as a way to simplify the circuit architecture and hence improve the performance. For performance validation, Tanner simulations were conducted on FAs implemented with TSMC 018 CMOS process technology in aspects of power consumption, delay time In contrast to other types of FAs with drivability, an GDI is superior to the other ones and can be applied to design related adder-based portable electronic products in practical applications in today's competitive markets.

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