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AN ANALYSIS AND SURVEY OF MULTILEVEL INVERTERSTOPOLOGIES, CONTROLS, AND APPLICATIONS

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ABSTRACT:

This paper includes different topologies of a multilevel inverter (MLI)The main purpose of this paper is to design multilevel inverter using different topologies. The various inverter topologies are Cascaded H-bridge inverter, Diode clamped inverter and Flying capacitor inverter. Multilevel inverters are similar to the convectional inverters but their output is in staircase form which is nearly a sine wave. Multilevel inverter takes DC as input and provides AC as output. The main advantage of multilevel inverter is that they provide AC output with low Total Harmonics Distortion (THD) but their design is complex. This paper also includes simulation of inverter topologies.

Key words: comparison, cascaded multilevel inverters, harmonic distortion, multilevel inverter, modulation,reduced number of device topologies, voltage balance.

1. INTRODUCTION:

A power inverter is an electronic device or circuitry that changes direct current to alternating current. The input voltage, output voltage and frequency, and overall power handling depend on the design of specific device or circuitry. Inverters are used to synthesize the required AC output from DC source. However, there are many limitations regarding Thus, many types of inverter have been introduced. Generally, the most recognized type is PWM inverter [1].

PWM inverter type offers various advantages over other types of inverters such as continuous and linearcontrol of the output voltage as well as better harmonics elimination. Multilevel inverters include an arrayof power semiconductors devices and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches allows the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. Fig. 1 shows a schematic diagram of one phase leg of inverters with different numbers of levels, for which the action of the power semiconductors is represented by an ideal switch with several positions[2].

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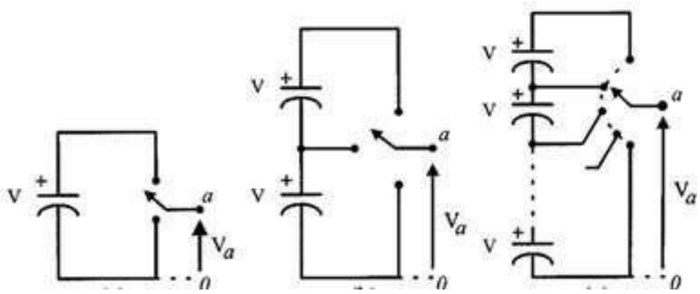

Fig.1. an Inverter with Two Levels, Three Levels and Multi Levels With One Phase

A two-level inverter generates an output voltage with two values (levels) with respect to the negative terminal of the capacitor [see Fig. 1.], while the three-level inverter generates three voltages, and so on. Multilevel voltage source inverter is an important alternative to the normal two level voltage source inverter especially in high voltage application. Using multilevel technique, the amplitude of the voltage is increased, stress in the switching devices is reduced and the overall harmonics profile is improved. Among the topologies, the most popular one is cascaded multilevel inverter. It exhibits several features such as simple circuit layout, less component count and avoid unbalance capacitor voltage problem. However, as the number of output level increases, the circuit becomes bulky due to the increase in the number of power devices. In this paper, it is proposed to employ a new technique to obtain a multilevel output using less number of power semiconductor switches when compared to ordinary cascaded multilevel inverter, which is suitable for renewable energy source interfacing. For higher-level operation, cascaded H-Bridge multilevel inverter are preferred but major disadvantage is requirement of multiple dc-sources, which is not feasible in many applications Voltage source converters are also required for various industrial applications, smart grid technologies etc. Due to high power requirement in these applications, using one power semiconductor switch directly is not advisable. For high power and medium voltage applications multilevel converters are introduced [2]. Using multilevel converters renewable energy sources can be easily interfaced to the grid. Using several low voltage DC sources such as capacitors, batteries and renewable sources with series power semiconductor switches high power converter can be achieved. These converters have several advantages over two level converters and can generate the output voltages with low distortion and less dv/dt stresses.

2. INVERTER TOPOLOGIES

The features of multilevel inverters are following:

1. These inverters can generate output voltages with extremely low distortion.
2. These inverters draw input current with very low distortion.
3. Using sophisticated modulation methods, CM voltages can be eliminated.
4. Multilevel inverters can operate with a lower switching frequency.

2.1. Diode-Clamped Inverter

As the name suggests, and unlike cascaded H-bridge inverters, they need clamping devices in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. Thus, the main concept of this inverter is to use diodes to limit the power devices voltage stress. A p level inverter needs **(**p-1) voltage sources, 2(p-1) switching devices and (p-1) (p-2) diodes. By increasing the number of voltage levels the quality of the output voltage is improved and the voltage waveform becomes closer to sinusoidal waveform. Figure.4 shows a three-level diode-clamped converter in which the dc bus consists of two capacitors, C1, C2. For dc-bus voltage V, the voltage across each capacitor is V/2 and each device voltage stress will be limited to one capacitor voltage level V/2 through clamping diodes. To explain how the staircase voltage is synthesized, the neutral point n is considered as the output phase voltage reference point. There are three switch combinations to synthesize three-level voltages across a and n.

Van=V/2, turn on the switches S1andS2. Van= 0, turn on the switches S2 and S1′.

Voltage level Van= - V/2 turn on the switches S1′, S2′.

A five-level diode-clamped converter in which the dc bus consists of four capacitors, C1, C2, C3, and C4. For dc-bus voltage V, the voltage across each capacitor is V/4 and each device voltage stress will be limited to one capacitor voltage level V/4 through clamping diodes**.**

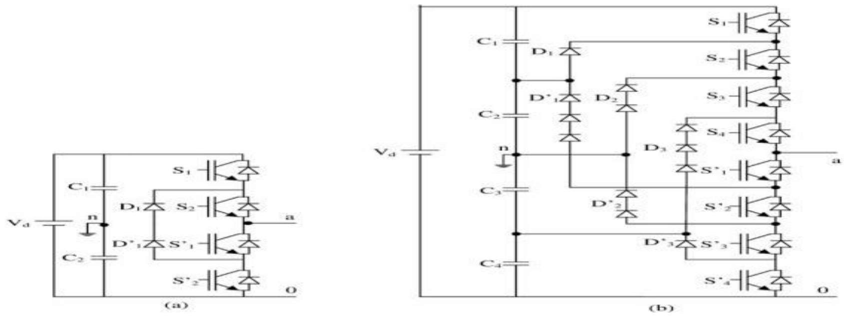

Fig.2: Diode-Clamped Multilevel (Three-Level & Five-Level) Inverter Circuit Topologies.

To synthesize 5-level output phase voltage, switching sequence as given in table 1. State condition 1 meansswitch ON and 0 means switch OFF**.**

Switch Combination Of Five Level Diode Clamped Inverter

Output Voltage Va0	Switch State							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S'_{a1}	S'_{a2}	S'_{a3}	S'_{a4}
Vdc/2	1	1	1	1	0	0	0	0
Vdc/4	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
-Vdc/4	0	0	0	1	1	1	1	0
Vdc/2	0	0	0	0	1	1	1	1

Table1: *Switching states in one leg of the five level diode clamped inverter level*

2.2. Cascaded Multilevel Inverter

One of the basic and well known topologies among all multilevel inverters is cascaded H-bridge multilevel Inverters. It can be used for both single and three phase conversion. The concept of this inverter is based on connecting H-bridge inverters in series to get a sinusoidal voltage output. The output voltage is the sum of the voltage that is generated by each cell. The switching angles can be

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chosen in such a way that the total harmonic distortion is minimized. One of the advantages of this type of multilevel inverter is that it needs less number of components i.e. it does not need any capacitors or diodes for clamping comparative to the Diode clamped or the flying capacitor, so the price and the weight of the inverter is less than that ofthe two types. Figure.3 shows the power circuit for one phase leg of a three-level and five-level cascadedinverter. In a 3-level cascaded inverter each single-phase full-bridge inverter generates three voltages at the output: +Vd, 0, -Vd (zero, positive dc voltage, and negative dc voltage). This is made possible by connecting the capacitors. The resulting output ac voltage swings from –Vd to +Vd with three levels, - 2Vd to +2Vd.

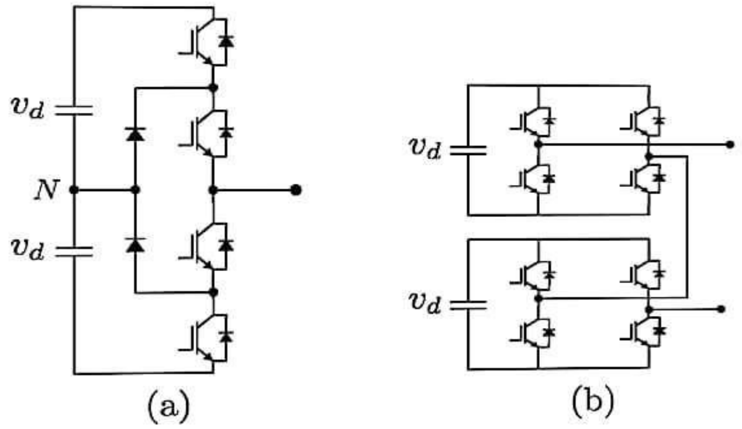

Fig.3: Single Phase Structures of Cascaded Inverter (A) 3-Level, (B) 5-Level

3. CAPACITOR CLAMPED INVERTER

A quite well known topology of multilevel inverter is capacitor clamped inverter. This type of multilevel inverter requires capacitor to be pre-charged. Capacitor clamped switching cells are connected in series. This topology has a ladder structure of dc side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform. Fig shows single phase n-level configuration of capacitor clamped inverter. A p-level inverter will require a total of (p-1) × (p-2)/2 clamping capacitors per phase leg in addition to (p-1) main dc bus capacitors. The voltage synthesis in a five-level capacitor-clamped converter has more flexibility than a diode- clamped converter. Using Figure.2 (b) the voltage of the five-level phase-leg “a” output with respect to the neutral point n (i.e. Van), can be synthesized by the following switch combinations.

1. Van= V/2, turn on all upper switches S1 - S4.
2. Van= V/4, there are three combinations.
3. Turn on switches S1, S2, S3 and S1′. (Van= V/2 of upper C4‟ s - V/4 of C1‟ s).
4. Turn on switches S2, S3, S4 and S4′.(Van= 3V/4 of upper C3‟ s - V/2 of C4‟ s).
5. Turn on switches S1, S3, S4 and S3′. (Van= V/2 of upper C4‟ s - 3V/4 or C3‟ s + V/2 of upper
6. Van= 0, turn on upper switches S3, S4, and lower switch S1′, S2′.
7. Van= -V/4, turn on upper switch S1 and lower switches S1′, S2′and S3′.
8. Van= -V/2, turn on all lower switches S1′, S2′, S3′ and S4′.

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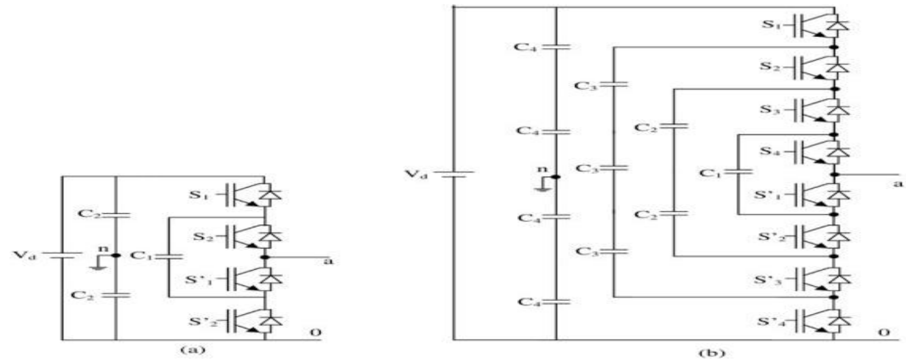

Fig.4: Capacitor-Clamped Multilevel Inverter Circuit Topologies, (A) 3-Level Inverter (B) 5-Level Inverter.

4. MULTILEVEL SINUSOIDAL PWM

Multilevel inverters generate stepped AC and use many number of switches and generate staircase type output through controlled switching. It is a popular control method widely used in inverter circuit. This method is easy to implement. The modulating signal is a sinusoid of frequency fm and amplitude Am. Atevery instant, each carrier is compared with the modulating signal.

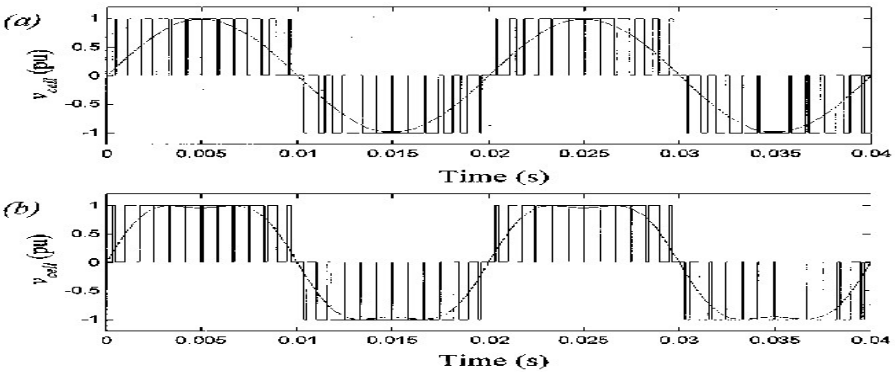

Figure.6: Inverter Cell Voltages. (A) Output Voltage and Reference with SPWM. (B) Output Voltage andReference with Injection of Sinusoidal Third Harmonic.

5. SPACE VECTOR MODULATION

Space vector modulation is an algorithm for control of pulse width modulation. It is used for creating of alternating current waveforms most commonly to drive 3-phase ac powered motors at varying speeds. One active area of development is in the reduction of total harmonic distortion created by rapid switching inherent to these algorithms. The basic idea of voltage space vector modulation is to control the inverter output voltages so that their Parks representation will be approximately equals the reference voltage vector. In the case of two level inverter, the output of each phase will be either +V/2 or – V/2. The SVM technique can be easily extended to all multilevel inverters. Figure.7 shows space vectors for the traditional two-, three-, and five-level inverters. These vector diagrams are universal regardless of the type of multilevel inverter. Space-vector PWM methods generally have the following features: good utilization of dc-link voltage, low current ripple, and relatively easy hardware implementation by a digital signal processor (DSP). These features make it suitable for high-voltage high-power applications. As the number of levels increases, redundant switching states

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and the complexity of selecting switching states increase dramatically**.**

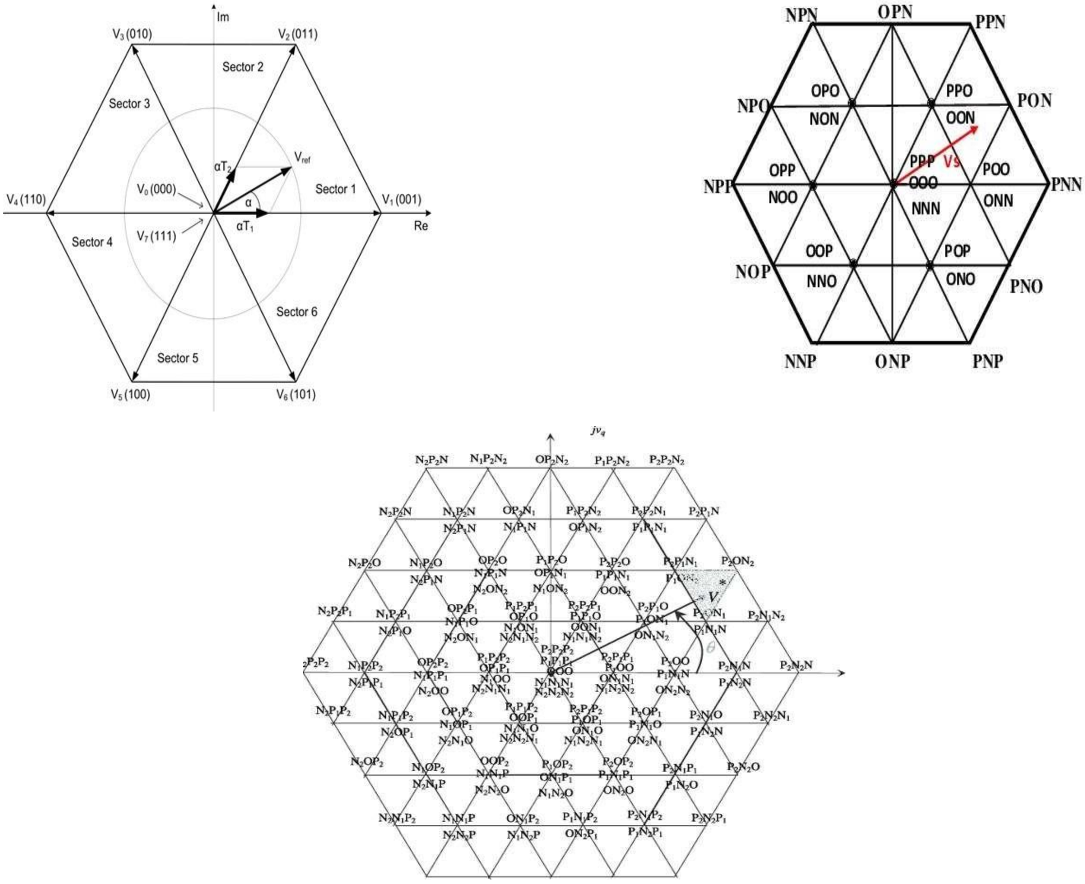

Figure.7: Space-Vector Diagram: (A) Two-Level, (B) Three-Level, and (C) Five-Level Inverter

6. A LITERATURES SURVEY WITH MULTI LEVEL INVERTER TOPOLOGIES ANDCONTROL TECHNIQUE

1. DIODE CLAMPED INVERTER 2.CASCADED MULTILEVEL INVERTER
3. FLYING CAPACITOR MULTILEVEL INVERTER
4. SINUSOIDAL PWM
5. SPACE VECTOR PWM
6. SHE-PWM
7. SPACE VECTOR CONTROL

6.1. Diode Clamped Inverter

The main concept of this inverter is to use diodes to limit the power devices voltage stress. A complete analysis of the voltage balance theory for a five-level back to- back system is given. This control strategy regulates the dc bus voltage, balances the capacitors, and decreases the harmonic components of the voltage and current. Robert Stala, et al. [3], introduced a new operational mode for diode-clamped multilevel inverters termed quasi two-level operation is proposed. Such operation avoids the imbalance problem of the dc-link capacitors for multilevel inverters with more than three levels.

6.2. Cascaded Multilevel Inverter

An arm-balancing control to achieve voltage balancing under all the operating condition is proposed. Farid Khoucha ,et al. [4], suggested the impacts of the connected load to the cascaded H-bridge converter as well as the switching angles on the voltage regulation of the capacitors are studied. This literature proves that voltage regulation is only attainable in a much limited operating conditions that it was originally reported.

6.3. Flying Capacitor Multilevel Inverter

Suroso, etal.[14], presented in this literature two active capacitor voltage balancing schemes are proposed for single-phase (Hybridge) flying-capacitor multilevel converters. They are based on the circuit equations of flying capacitor converters. These methods are shown to be effective on capacitor voltage regulation inflying- capacitor multilevel converters. The development of multilevel hysteresis current regulation strategies.

6.4. Sinusoidal PWM

Wahidah Abd. Halim, et al., [12], used an original multicarrier sub harmonic pulse width modulation (PWM), called disposition band carrier and phase-shifted carrier PWM (DBC-PSC-PWM).

6.5. Space Vector PWM

A new technique is proposed in this literature, by which these two-level vectors are translated to the switching vectors of the multilevel inverter by adding the center of the subhexagon to the two-level vectors. J. Selvaraj, et al. [8], presented in this literature an approach to reduce common-mode voltage (CMV) at the output of multilevel inverter using 3-D space-vector modulation (SVM). N. A. Rahim, et al. [8], addressed a new multilevel SVPWM technique with a five-segment switching sequence, where half- wave symmetrical PWM voltage waveforms are used to balance the inductor common-mode dc voltages.

6.6. She-PWM

Ilhami Colak, et al., focused on a new formulation of selective harmonic elimination pulse width modulation (SHE-PWM) technique suitable for cascaded multilevel inverters with optimized DC voltagelevels. Jorge Pontt, et al., introduced a neutral point voltage control strategy for the three-level active neutral point clamped (ANPC) converter using selective harmonic elimination pulse width modulation (SHE-PWM). Jorge Pontt ,et al., presented in this literature a control strategy is proposed to regulate the voltage across the FCs at their respective reference voltage levels by swapping the switching patterns ofthe switches based on the polarity of the output current.

6.7. Space Vector Control

José Rodríguez, et al., addressed a switching strategy for multilevel cascade inverters, based on the space-vector theory. The proposed switching strategy generates a voltage vector with very low harmonic distortion and reduced switching frequency. J. S. Lai,et al[1], used a new PWM technique for induction motor drives involving six concentric dodecagonal space vector structures is proposed. José Rodríguez, et al., introduced a switching strategy for multilevel cascade inverters, based on the space-vector theory.

7. CONCLUSION

The following tables give conclusion of the paper as:

The Conclusion 28.27 % of total literatures are reviews based on Diode Clamped Multilevel Inverter,

39.09 % of total literatures are reviews based on Cascaded H-bridge Multilevel Inverter, 32.70 % of totalliteratures are reviews based on Flying Capacitor Multilevel Inverter viewpoints.

Multilevel Inverter Topologies Point of View

Parameters	**Total No. of Literatures Reviews (44)**	**% of Literatures (44)**
Diode clamped	12	28.27
Cascaded H -bridge	18	39.09
Flying Capacitor	14	32.70

7.1. Modulation Strategies Point of View

From below tables 3, it is concluded that the 26.32 % of total literatures are reviews based on Sinusoidal PWM Technique, 28.95 % of total literatures are reviews based on Space Vector PWM Technique, 34.21% of total literatures are reviews based on Selective Harmonic Elimination PWM Technique and 10.52 % of total literatures are reviews based on Space Vector Control Technique viewpoints.

Parameters	**Total No. of Literatures Reviews (44)**	**% of Literatures (44)**
SPWM	10	26.99
SVM	11	29.09
SHE-PWM	13	35.71
SVC	4	11.20

Table: 3 *Modulation Strategies Point of View*

From above tables 3, it is concluded that the 26.99% of total literatures are reviews based on Sinusoidal PWM Technique, 29.09 % of total literatures are reviews based on Space Vector PWM Technique, 35.71% of total literatures are reviews based on Selective Harmonic Elimination PWM Technique and 11.20 % of total literatures are reviews based on Space Vector Control Technique viewpoints.

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